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MT 6630T Application Note

Version : V03

Agenda

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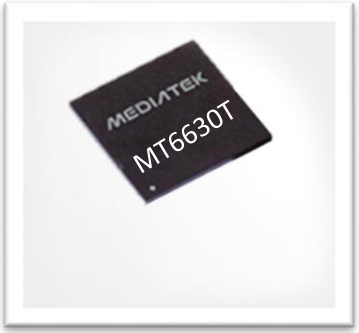
Section 1.
HW system overview

Version : V03

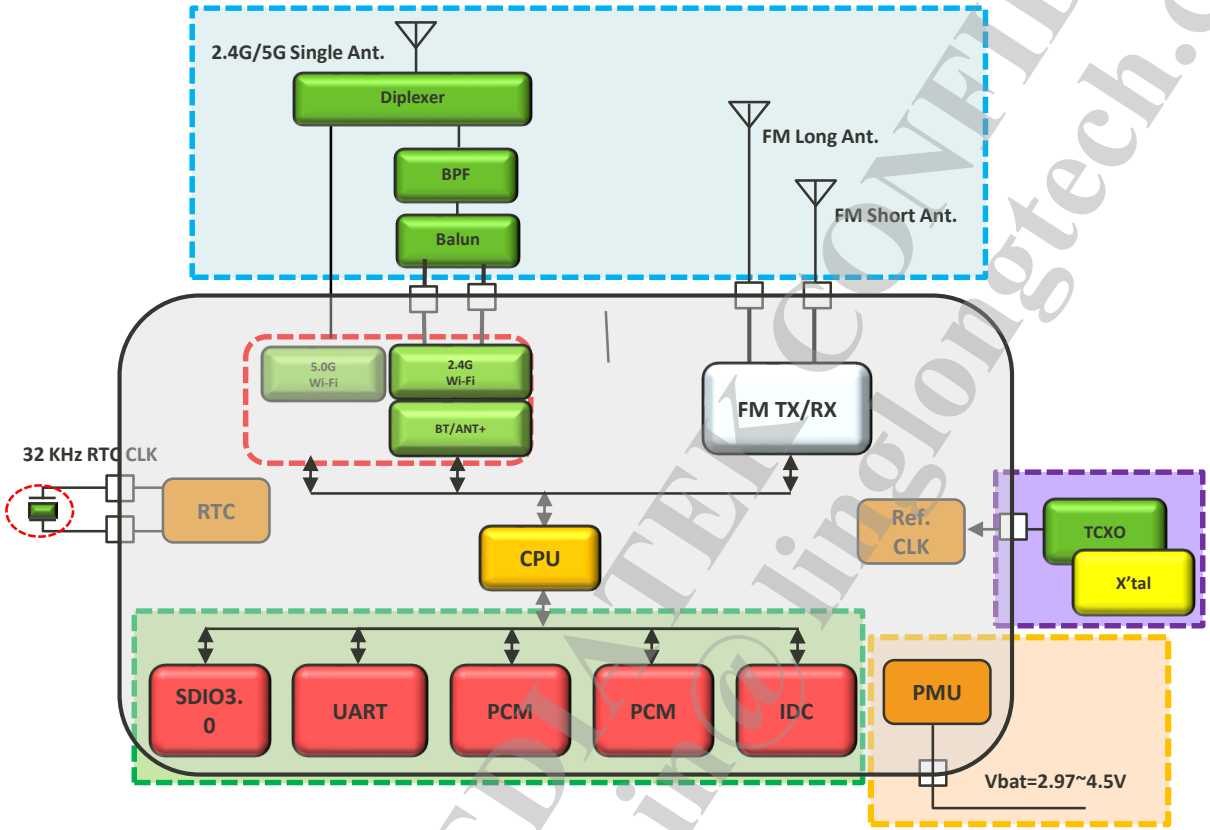
MT6630T Product Overview

Product Availability	
Process	55nm CMOS
Package	WLCSP 5.013x5.013 mm² ; QFN 7x7 mm²
Schedule	ES Dec'13; MP Mar'14
Interface	SDIO 3.0, UART, PCM, I2S, Line In/Out
Feature Highlights	
WLAN	• 802.11abgn/ac 1T1R up to 210Mbps throughput • Integrated Wi-Fi 2.4G PA (Max 23dBm), 5G PA (Max 18.5dBm), LNA, TRSW • 4T1R Beamformee, STBC, LDPC, MU-MIMO Rx
BT	• BT 3.0+HS, BT 4.1 LE • Integrated 12dBm PA, TRSW • Lowest sensitivity -95dBm (GFSK)
ANT+	• The wireless protocol standard for sport and fitness monitors • Similar RF performance as BT block
FM	• FM Transmitter and Receiver • 65-108MHz with 50KHz step • FM Tx Max output power 120dBuV • Short antenna support



ES: Dec 2013
MP: Mar 2014

MT6630T System Block Diagram



◆ FE

1.1.5G/2.4G/5G single ant.
2.LTE co-existence filter
3.5G Ext. FEM support
4.FM LANT/SANT

◆ Clock

1. TCXO
2. Crystal

◆ PMU

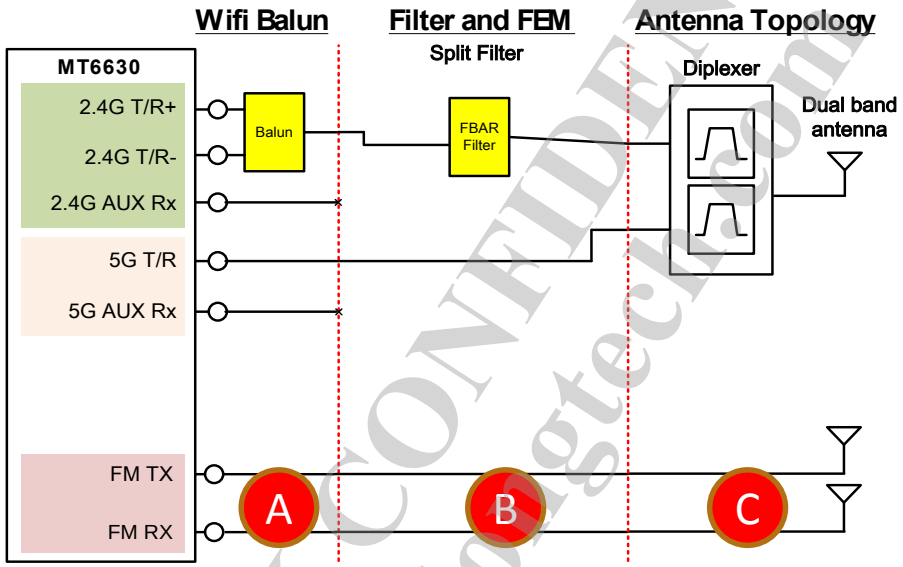
1. SIDO buck convertor (1.2V/1.5V)
2. PALDO (3.3V)
3. ALDO (2.8V)

◆ Interface

1. I2S (FM)
2. Audio LIN/LOUT (FM)
3. DAI/PCM (BT, FM)
4. SDIO2.0/3.0
5. UART
6. IDC (LTE Co-existence)

MT6630TQ RF Front-end Architectures

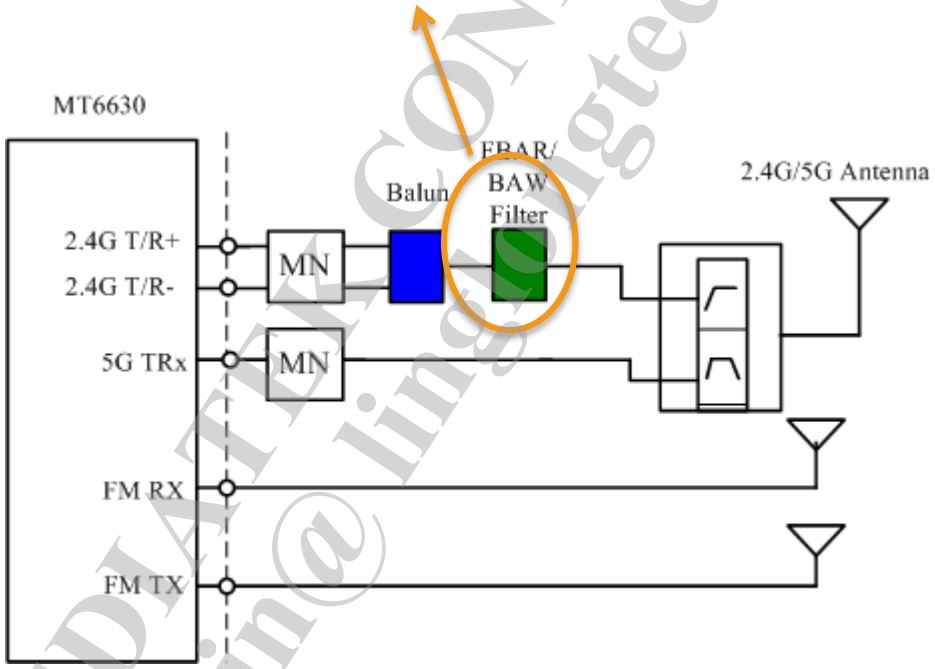
With LTE Platform



A Wifi Balun	B Filter and FEM	C Antenna Topology
1. **2.4G Balun (Main):** • LTE co-existence 2. **2.4G Balun Filter:** • GSM/WCDMA case only	**Filter** 1. **BAW/FBAR Filter:** • LTE to 2370M platform 2. **None:** • GSM/WCDMA case only	1. **Single Ant. (Main):** • Wifi 2.4G/5G with Diplexer 2. **Dual Ant.:** a. 2.4G/5G with diplexer b. 2.4G/5G RX diversity

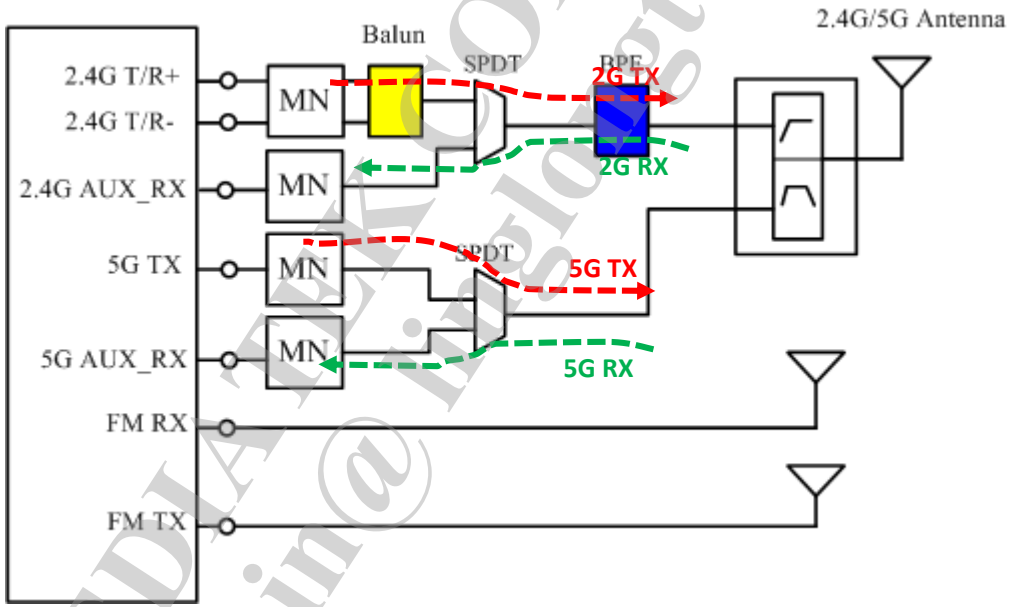
MT6630T Front End Architecture (I)

- **Main front- end solution**
  - 2G_5G WiFi/BT single antenna.
  - Diplexer for 2.4G/5G band selection.
  - 2.4G BPF selection
    - With Bal-filter for coexistence with GSM/WCDMA.
    - With FBAR/BAW filter for coexistence with LTE.



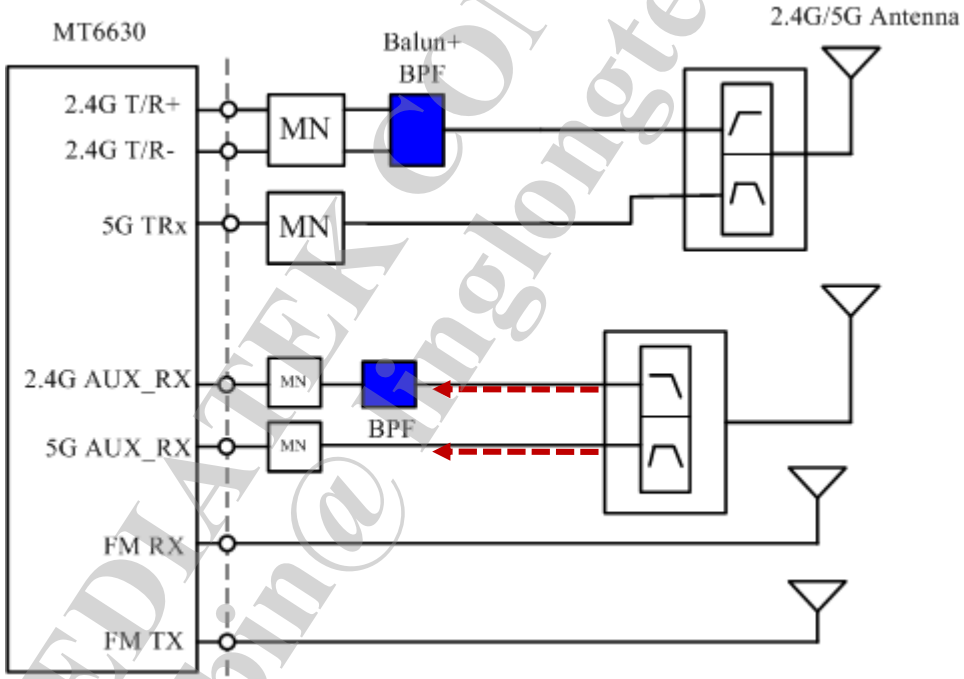
MT6630T Front End Architecture (II)

- **AUX-RX front- end solution**
  - WiFi High-sensitivity performance.
  - Need 2 extra T/R switch
  - 2G_5G WiFi/BT single antenna.
  - Diplexer for 2.4G/5G band selection.



MT6630T Front End Architecture (III)

- **WiFi RX diversity front- end solution**
  - Support WiFi 2G/5G dual band RX diversity antenna
  - 2G_5G WiFi/BT single antenna.
  - Diplexer for 2.4G/5G band selection.



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Section 2.
Build-in Power Manager Unit

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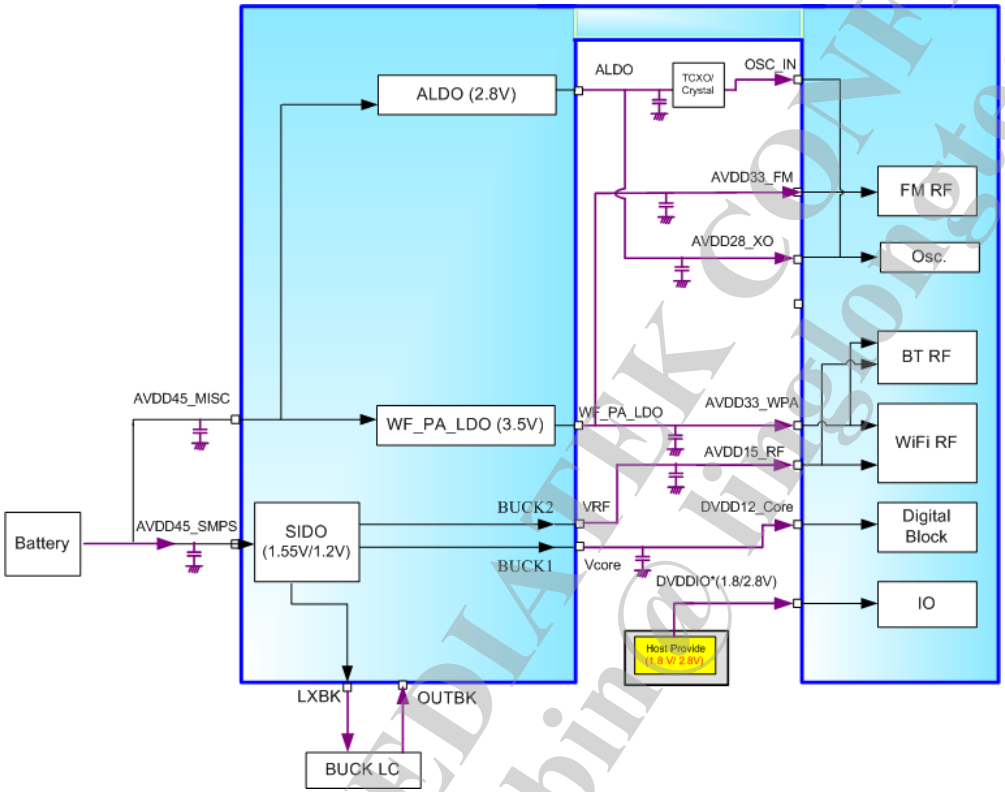
MT6630T PMU Power Scheme

- Vbat operation range is 2.97V~4.5V.
- Built-in power manager unit including high efficiency DC to DC, digital LDO and analog LDO.
- Innovative SIDO architecture design to effectively reduce power consumption and increase battery life.

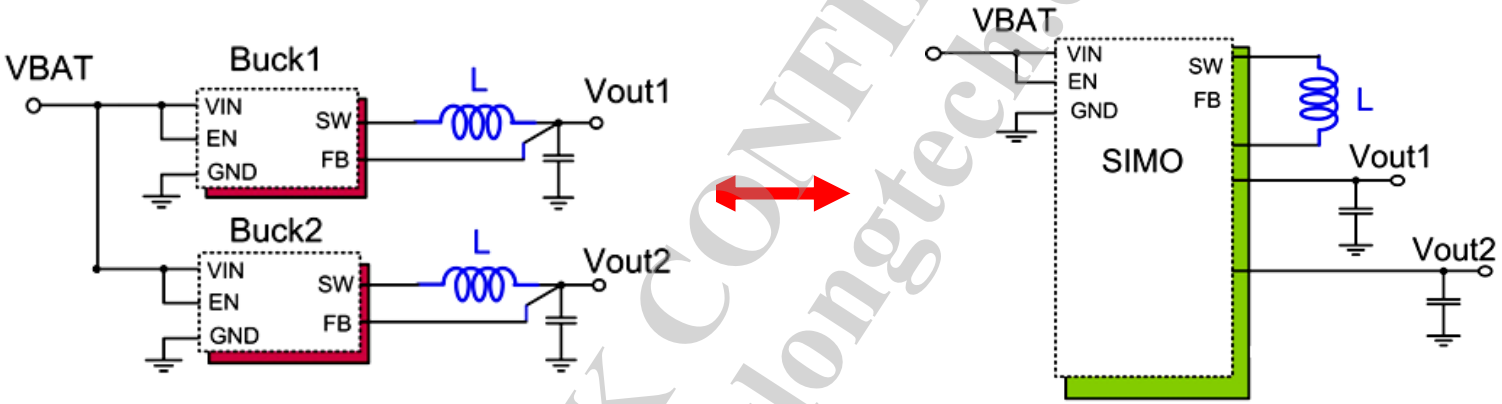


PMU	Sub-block	Vout	Max current	Efficiency (Typ.)
BUCK1	Core	1.2V	420mA	82%
BUCK2	RF AFE	1.5V	280mA	82%
PALDO	WiFi/BT PA FM RF	3.5V	450mA	-
ALDO	TCXO/	2.8V	30mA	-

MT6630T PMU SIDO Design

SIDO – Single In Dual Output

- Cost reduction and simplify layout constrain.
- Effectively increasing PMU overall efficiency



Sharing the storage element: inductor

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Section 3.
HW Interface Design

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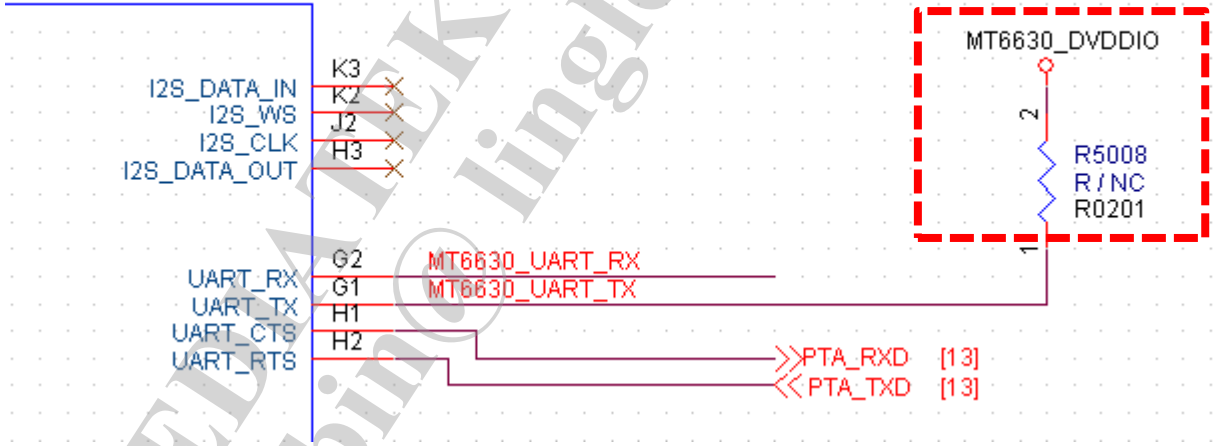
MT6630T Host interface

- Except SDIO interface, MT6630T also support Host UART interface for BT/FM application.
- Default host interface is common SDIO, if using UART+SDIO I/F, please adding 10K Pull-up resister for UART mode strap.

	Host Interface	UART_TXD
BT/FM Host Interface	SDIO (Default)	0
	UART	1

- 10K Pull-Up RES. for UART interface
- "NC" for Common SDIO



MT6630T I/O Power Domain

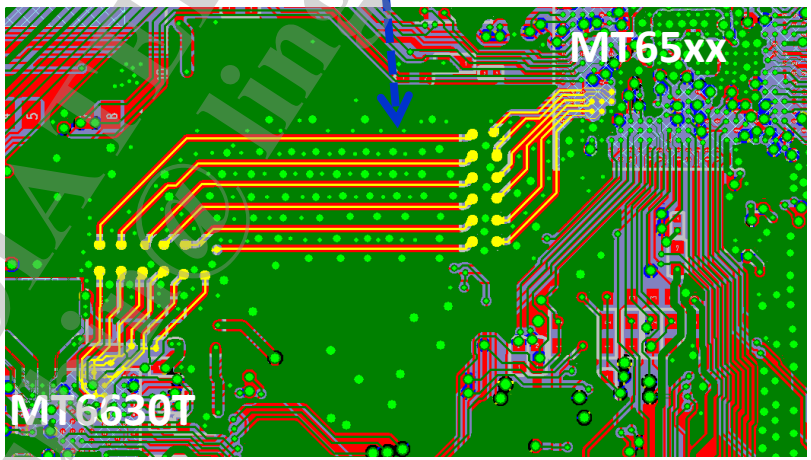
MT6630T I/O power domain is listed as following table.

Power	Pin Name	Direction (reset)	
		Duration	After
DVDDIO (1.8V/2.8V/3.3V)	SYSRST_B		
DVDDIO (1.8V/2.8V/3.3V)	BOND_OPTION		
DVDDIO (1.8V/2.8V/3.3V)	OSC_EN		
DVDDIO (1.8V/2.8V/3.3V)	WIFI_INT_B(W) / GPIO0(Q)		
DVDDIO (1.8V/2.8V/3.3V)	BGF_INT_B		
DVDDIO_SDIO(1.8V/2.8V)	SDIO_CLK		I
DVDDIO_SDIO(1.8V/2.8V)	SDIO_CMD		I/O
DVDDIO_SDIO(1.8V/2.8V)	SDIO_DAT3		I/O
DVDDIO_SDIO(1.8V/2.8V)	SDIO_DAT2		I/O
DVDDIO_SDIO(1.8V/2.8V)	SDIO_DAT1		I/O
DVDDIO_SDIO(1.8V/2.8V)	SDIO_DAT0		I/O
DVDDIO (1.8V/2.8V/3.3V)	UART_RX		I / PU
DVDDIO (1.8V/2.8V/3.3V)	UART_TX	I/PU	O / PU
DVDDIO (1.8V/2.8V/3.3V)	UART_RTS		O / PU
DVDDIO (1.8V/2.8V/3.3V)	UART_CTS		I / PU
DVDDIO (1.8V/2.8V/3.3V)	PCM_CLK		I/O / PD
DVDDIO (1.8V/2.8V/3.3V)	PCM_SYNC		I/O / PD
DVDDIO (1.8V/2.8V/3.3V)	PCM_OUT		O / PD
DVDDIO (1.8V/2.8V/3.3V)	PCM_IN		I / PD
DVDDIO (1.8V/2.8V/3.3V)	I2S_CLK		
DVDDIO (1.8V/2.8V/3.3V)	I2S_WS		
DVDDIO (1.8V/2.8V/3.3V)	I2S_DATA_OUT	I/PD	
DVDDIO (1.8V/2.8V/3.3V)	I2S_DATA_IN		
DVDDIO (1.8V/2.8V/3.3V)	FM_LOUT (GPIO2)		
DVDDIO (1.8V/2.8V/3.3V)	FM_ROUT (GPIO3)		
DVDDIO (1.8V/2.8V/3.3V)	RFPD5G		
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	RFPD2G		
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	ANTSEL0	I / PD	O / PD
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	ANTSEL1	I / PD	O / PD
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	ANTSEL2	I / PD	O / PD
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	ANTSEL3	I / PD	O / PD
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	ANTSEL4	I / PD	O / PD
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	ANTSEL5	I / PD	O / PD
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	ANTSEL6	I / PD	O / PD
DVDDIO_ANTSEL (1.8V/2.8V/3.3V)	ANTSEL7	I / PD	O / PD

SDIO3.0 Layout Guide

- MT6630T support SDIO3.0, the max. clock rate of SDIO3.0 is up to 208MHz.
- For high speed interface, the timing of signal is quite critical. Good SDIO3.0 PCB layout can avoid the unexpected signal timing issue.
- MTK strongly recommend that SDIO3.0 PCB layout **MUST** obey following rules.

	PCB layout Rule
SDIO 3.0 MT6630T	Trace 長度限制4000mil CLK,CMD,DATA 每條線兩邊包地 需要有GND參考層 若分層走線上下不可重疊 留測點 (option) 穿層越少越好 **走線誤差300mil**



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Section 4.
WiFi/BT/FM Application circuit design

Version : V03

MT6630T WiFi Part Design Notice

Version : V03

MT6630T Wifi Feature and Performance

- 2.4G/5G dual band RF
- Support 802.11 a/b/g/n/ac.
- SDIO 3.0 host interface with 200MHz clock rate.
- 2.4G performance table:

WiFi				
Item	Condition	MT6630T	MT6628	Unit
Rx current	2.4GHz, 1Mbps	44.9	44	mA
Rx current	2.4GHz, 54Mbps	52.1	48.1	mA
Rx current	2.4GHz, HT20 MCS7	53.2	47.4	mA
Rx current	2.4GHz, HT40 MCS7	59.1	57	mA
Rx current	Listen	47.7	41.3	mA
Rx current	Sleep	0.1	0.106	mA
Rx current	Power Saving, DTIM=1	0.59	0.56	mA
Tx current	2.4GHz, 1Mbps, 23dBm	292.5	210*	mA
Tx current	2.4GHz, 54Mbps, 20dBm	251.9	185*	mA
Tx current	2.4GHz, HT20 MCS7, 19.5dBm	224.7	172.5*	mA
Tx current	2.4GHz, HT40 MCS7, 18.5dBm	229	181*	mA

WiFi	Test @ Chip in/out			
Item	Condition	MT6630T	MT6628	Unit
Rx sensitivity	2.4GHz, 1Mbps	-99	-98.5	dBm
Rx sensitivity	2.4GHz, 11Mbps	-90	-91	dBm
Rx sensitivity	2.4GHz, 6Mbps	-95.5	-95	dBm
Rx sensitivity	2.4GHz, 54Mbps	-78	-77.5	dBm
Rx sensitivity	2.4GHz, HT20 MCS7	-76.5	-75.5	dBm
Rx sensitivity	2.4GHz, HT40 MCS7	-73	-72	dBm
Tx power	2.4GHz, 1Mbps	23	21	dBm
Tx power	2.4GHz, 11Mbps	23	21	dBm
Tx power	2.4GHz, 6Mbps	20	18	dBm
Tx power	2.4GHz, 54Mbps	20	18	dBm
Tx power	2.4GHz, HT20 MCS7	19.5	18	dBm
Tx power	2.4GHz, HT40 MCS7	18.5	16	dBm

MT6630T Wifi Feature and Performance

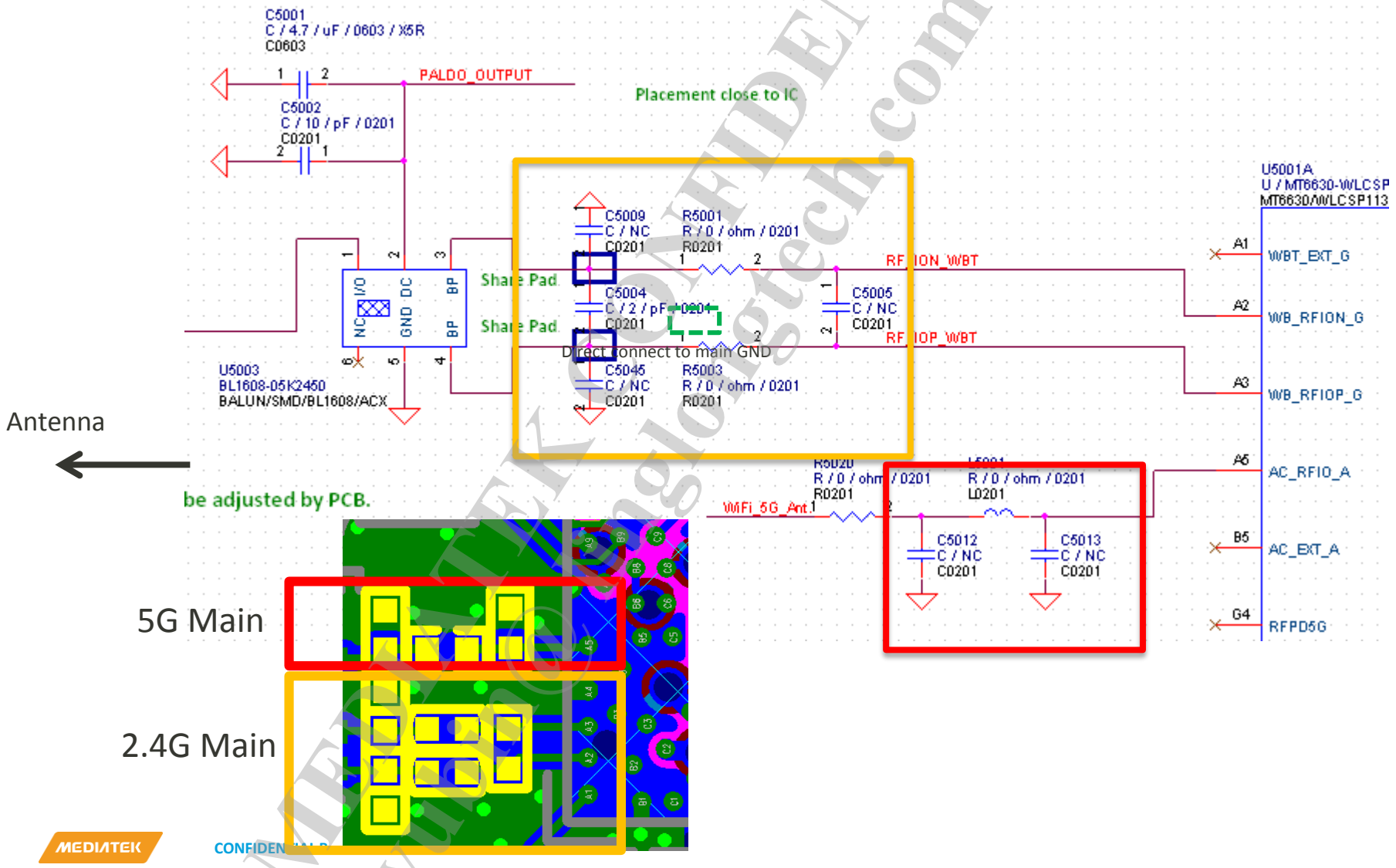
- **5G performance table:**

WiFi			
Item	Condition	MT6630T	Unit
Rx current	5GHz, 6Mbps	71.3	mA
Rx current	5GHz, 54Mbps	71.5	
Rx current	5GHz, VHT20 MCS8	73.5	mA
Rx current	5GHz, VHT40 MCS9	73.4	mA
Rx current	5GHz, VHT80 MCS9	93.5	mA
Rx current	Listen		mA
Rx current	Sleep		mA
Rx current	Power Saving, DTIM=1		mA
Tx current	5GHz, 6Mbps, 18.5dBm	370.4	mA
Tx current	5GHz, VHT20 MCS7	359	mA
Tx current	5GHz, VHT40 MCS9, 16dBm	354	mA
Tx current	5GHz, VHT80 MCS7, 16dBm	359	mA

WiFi	Test @ Chip in/out		
Item	Condition	MT6630T	Unit
Rx sensitivity	5GHz, 6Mbps	-95.5	dBm
Rx sensitivity	5GHz, 54Mbps	-78	dBm
Rx sensitivity	5GHz, VHT20 MCS8	-71.5	dBm
Rx sensitivity	5GHz, VHT40 MCS9	-67	dBm
Rx sensitivity	5GHz, VHT80 MCS9	-63	dBm
Tx power	5GHz, 6Mbps	18.5	dBm
Tx power	5GHz, 54Mbps	18.5	dBm
Tx power	5GHz, VHT20 MCS7	17.5	dBm
Tx power	5GHz, VHT40 MCS9	16	dBm
Tx power	5GHz, VHT80 MCS9	16	dBm

WiFi Front-end Schematic

- Please follow the matching topology for Wifi 2G and 5G port.



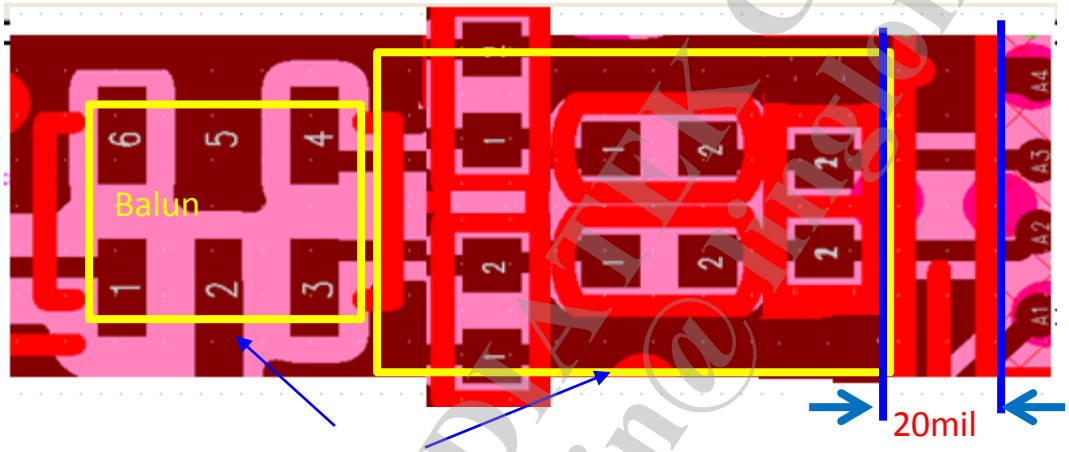
2.4G WiFi/BT Front-end layout guide

❑ Background

- 2.4G Wifi and BT share the same RF port. The key performance factors like EVM, TX power and spectrum are sensitive to the front-end layout.
- Please follow MT6630T layout guideline which can guarantee the mass production quality and yield to our customers.

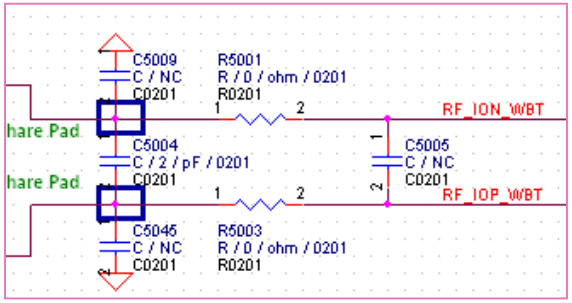
❑ MT6630T Front-end matching network layout guide:

1.RF differential trace 100 Ohm. The differential trace from IC to matching component should be straight, symmetry and equal length.
2.RF trace after balun is a 50 Ohm line with solid GND VIAs in nearby GND plane
3.Do not put any VIAs under the RF trace
4.Matching components are 0201 size
5.Keep the distance of matching component group to IC outline is 20mil
6.Balun and matching components should as close as possible to MT6630T IC

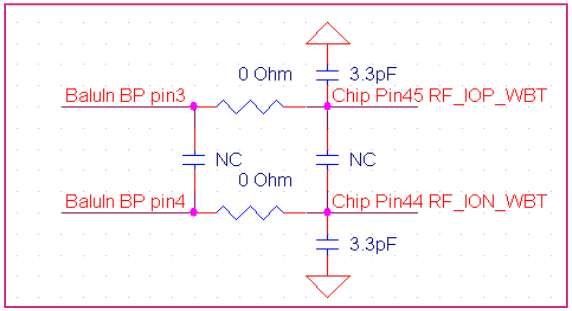


Keep balun, matching network and 6630 chip as close as possible

WLCSP package Matching Circuit reference value:

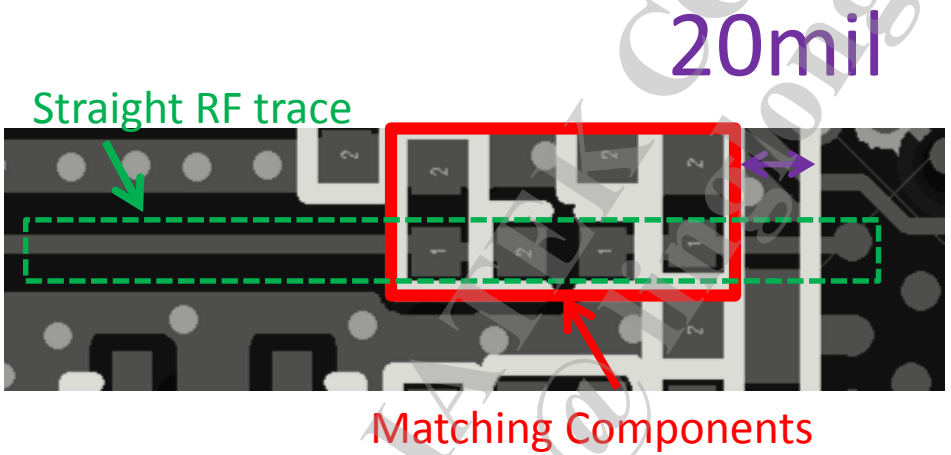


QFN package Matching Circuit reference value:

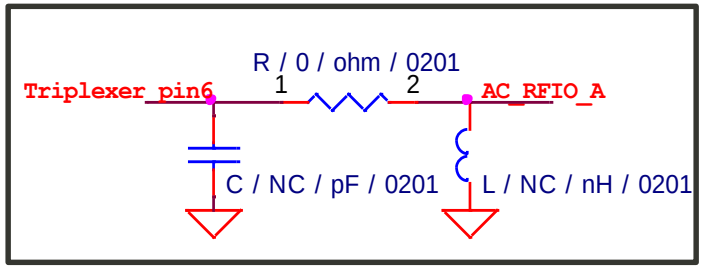


5G Wifi RF Layout Guideline

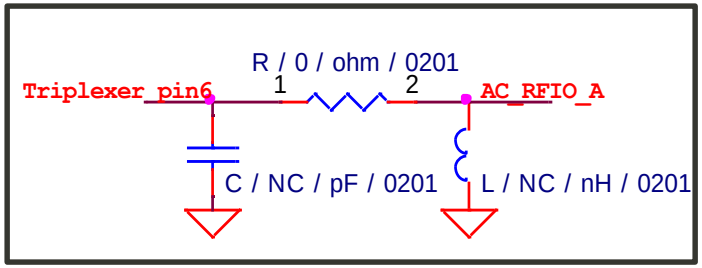
1. **Do not** put VIAs under RF trace and nearby IC A5/B5 balls.
2. Keep 5G RF trace as a **straight line**. Follow reference layout.
3. To Routing RF trace on **PCB surface layer** (the same side with MT6630T) and don't cross inner layers.
4. Matching components are 0201 size and put them close to IC (**20mil**)
5. RF trace rule:
   - RF trace: 50 Ohm with solid GND VIAs in nearby GND plane



WLCSP package Matching Circuit reference value:

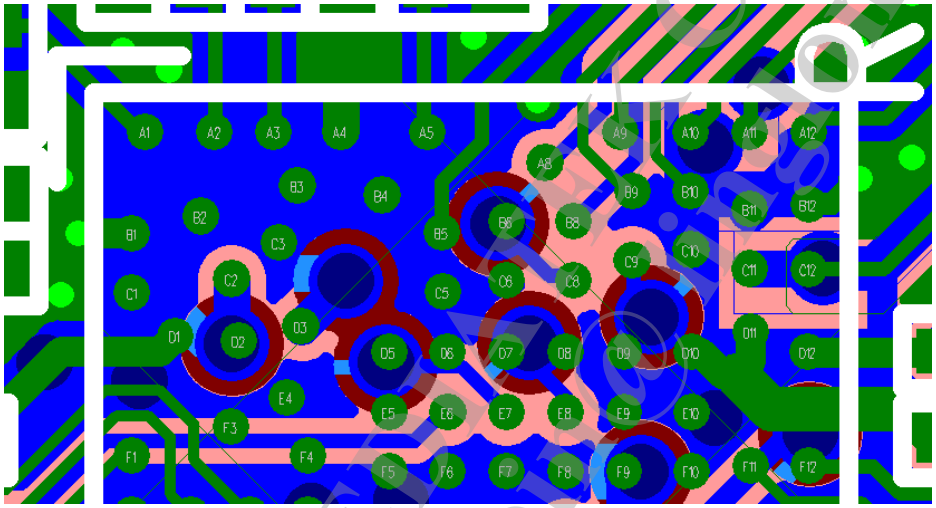


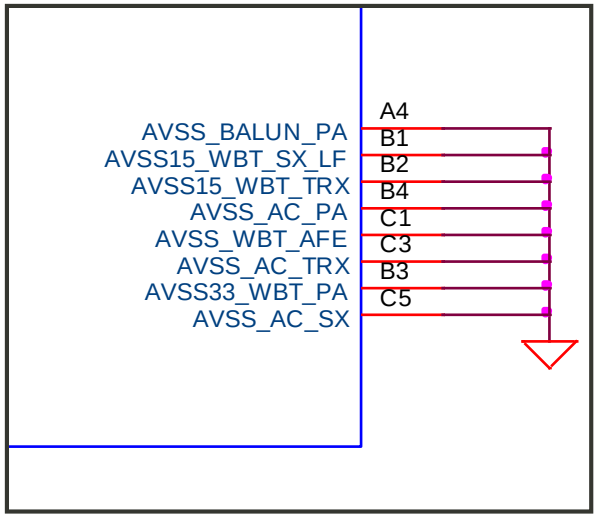
QFN package Matching Circuit reference value:



GND Plane around Wifi RF Part

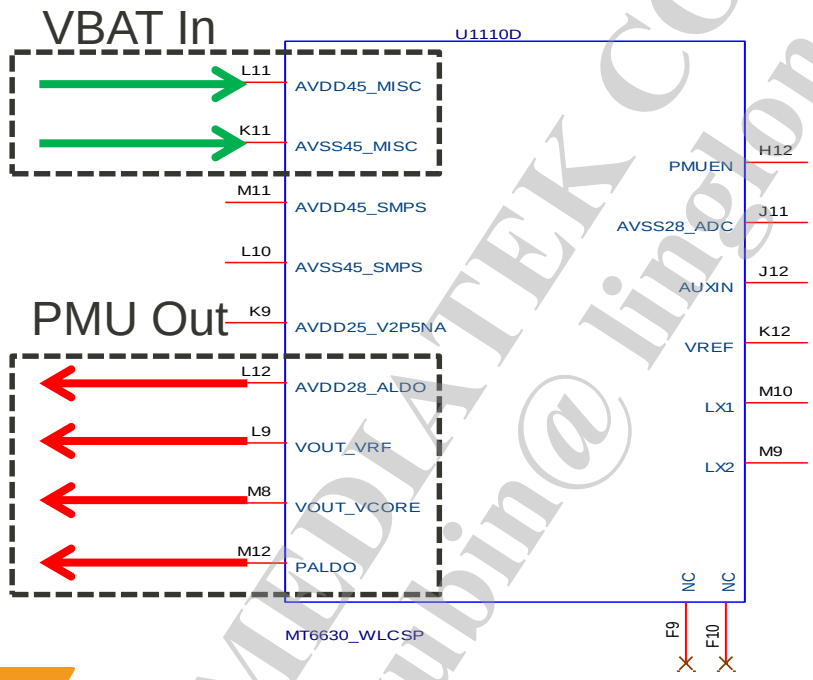
1. Do not connect the GND balls together by L1 trace. Please keep them separate and directly connect to L2 GND. (A4, B1, B2, B3, B4, C1, C3,C5)
2. Do not add GND VIAs near RF trace.
3. Keep L2 be a good GND plane nearby Wifi RF part.

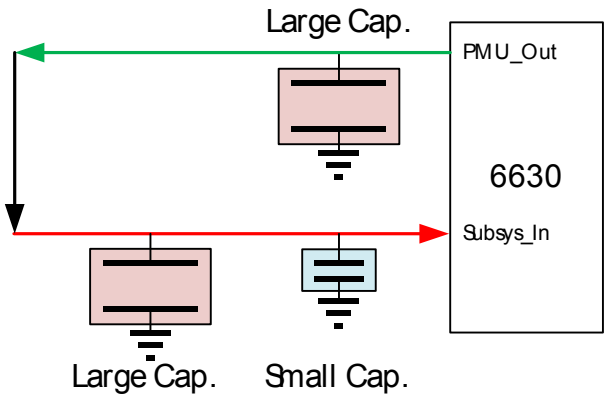




PMU Part

- **PMU related layout placement**
  - **When doing placement, please follow the rule below**
    1. **Capacitors should be close to IC pins.**
    2. **Be careful the current direction and capacitor placement position.**

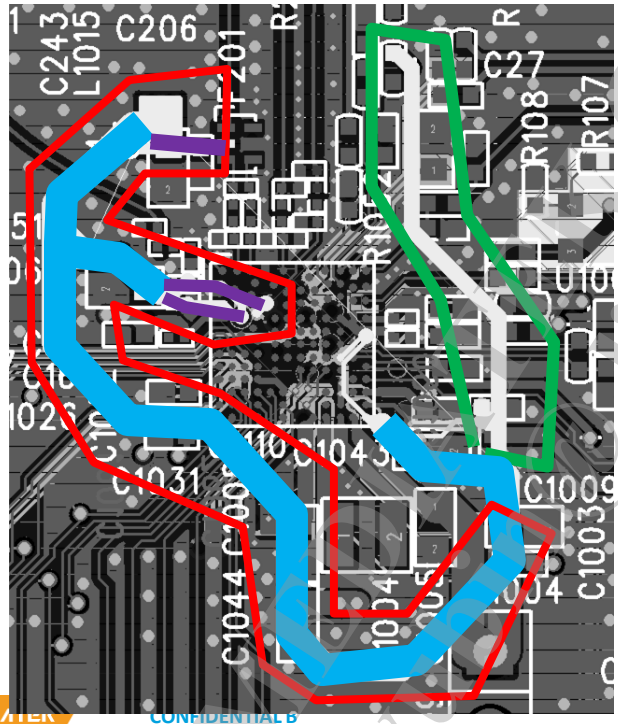




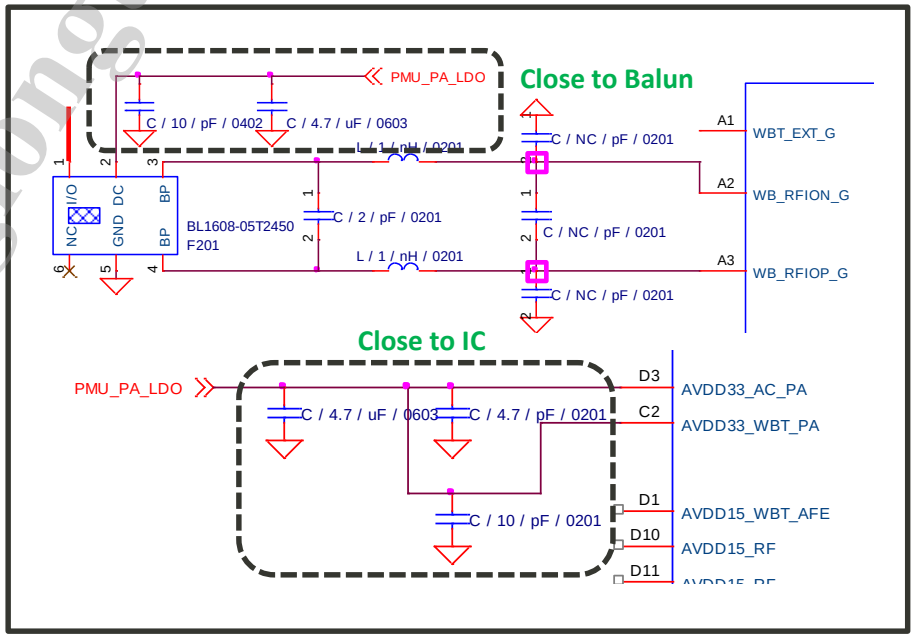
Wifi Related Power: PMU_PALDO (1/3)

- **PMU__PALDO to AVDD33_AC_PA, AVDD33_WBT_PA and Balun (2.4G PA)**
  1. Put 5G decoupling capacitors close IC and 2.4G close to balun. Solid GND plane and enough GND VIAs are needed for PALDO decouple capacitors
  2. The PMU_PALDO trace width should be 30mil (recommend) not less than 20mil because of large current flow (Blue line). PMU_PALDO close to IC should not less than 12mil (Purple line).
  3. Separate connection with AVDD33_FM

PALDO: AVDD33_FM branch



PALDO: Wifi PA branch



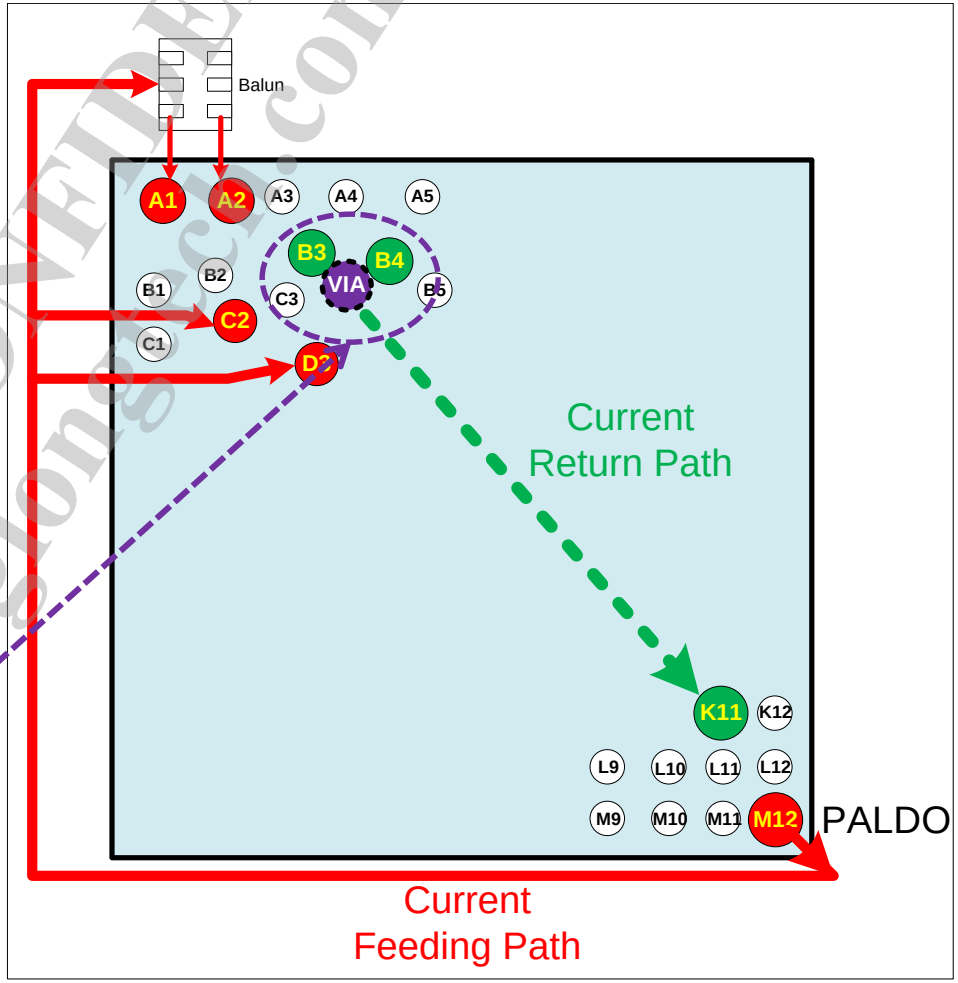
Wifi Related Power: PMU_PALDO (2/3)

- **For a better Wifi PA performance, DC grounding is as crucial as the RF grounding.**

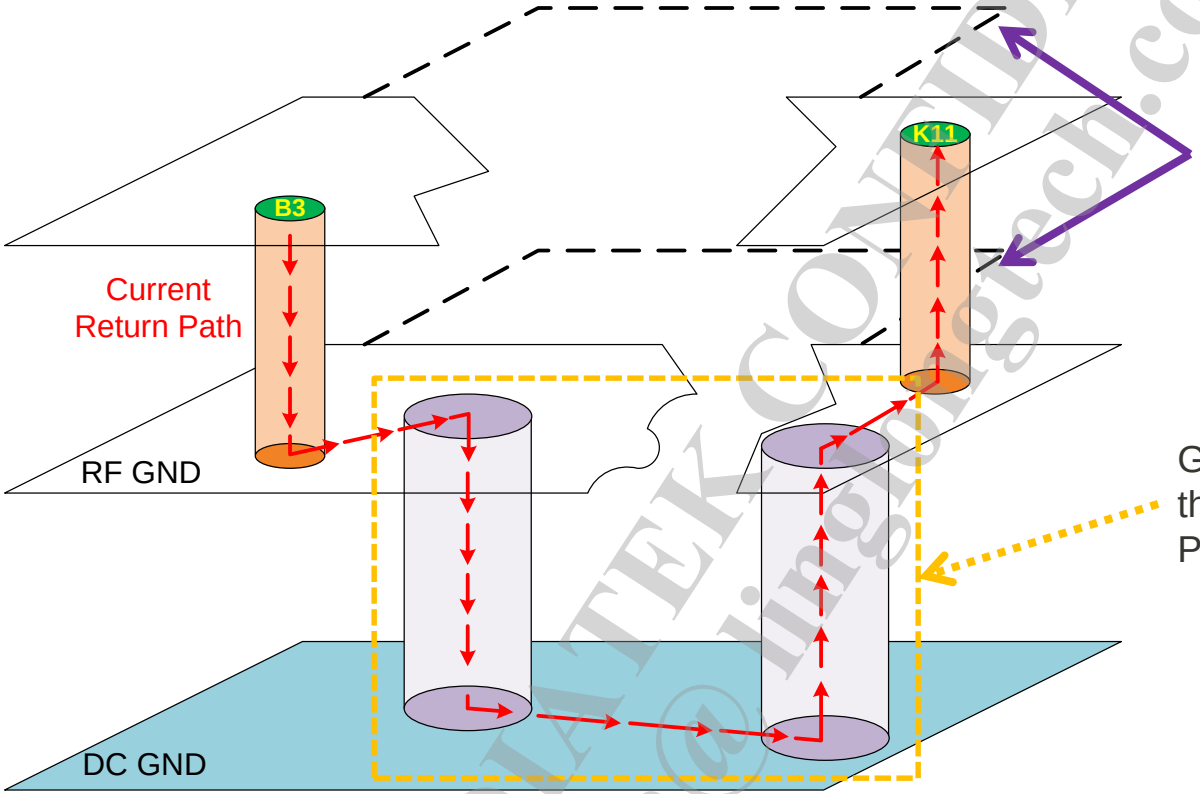
1. **Be careful of the DC current path. Wrong DC current return path may cause unexpected signal coupling.**

2. **Weak PA GND makes ground bouncing.**

3. **B3 and B4 are 2.4G and 5G wifi PAs' GND point. Please make sure there's a strong GND VIA near B3 and B4.**



Wifi Related Power: PMU_PALDO (3/3)

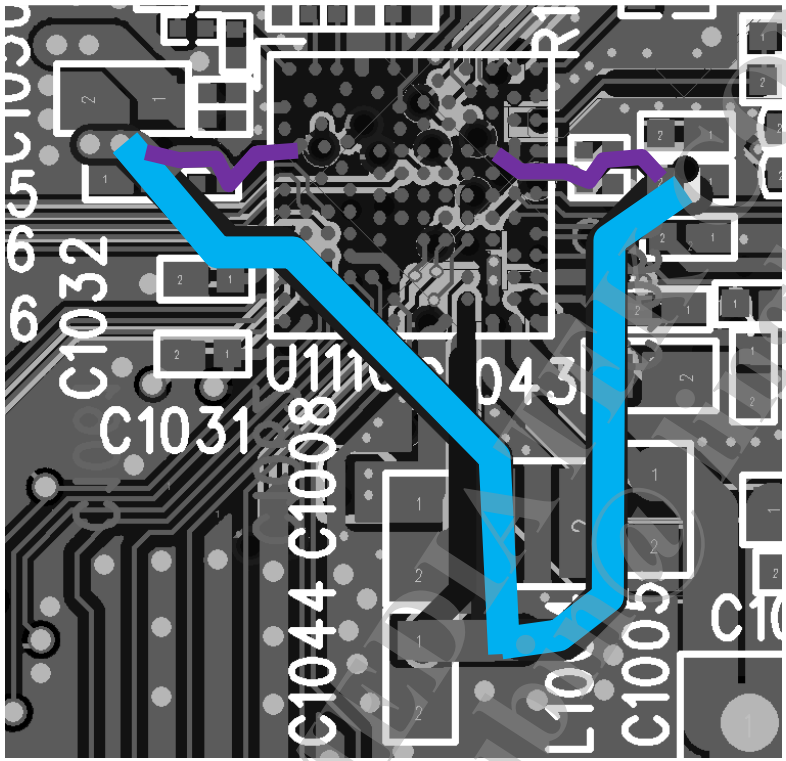


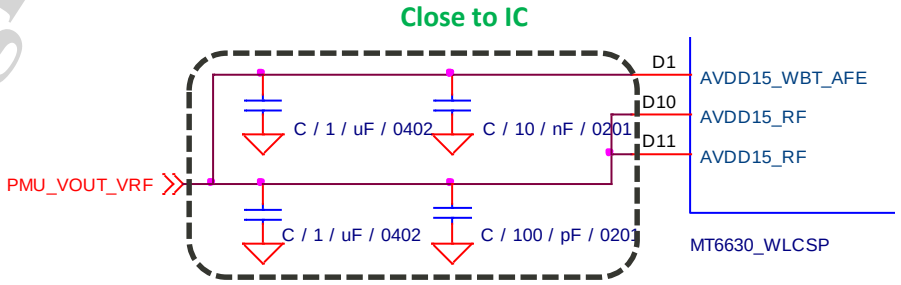
Because of L1 and L2 GND is fragmented (large impedance for DC return current). The solid L3 GND plane is the best way for return current

GND VIA puts near B3 and B4 can lead the return current in right direction to the PMU GND.

Wifi Related Power: PMU_VRF

- **PMU_VRF to AVDD15_RF and AVDD15_WBT_AFE**
  1. Routing trace width is 20mil (recommend) not less than 15mil (Blue line) . PMU_VRF close to IC should not less than 10mil (Purple line).
  2. The trace should be protected by GND carefully. Separate from other large current power lines (PMU_Vcore or PMU_PALDO) and digital IO signals.
  3. Decoupling capacitors should be lose to IC power pins





MT6630T BT Part Design Notice

Version : V03

BT Performance overview

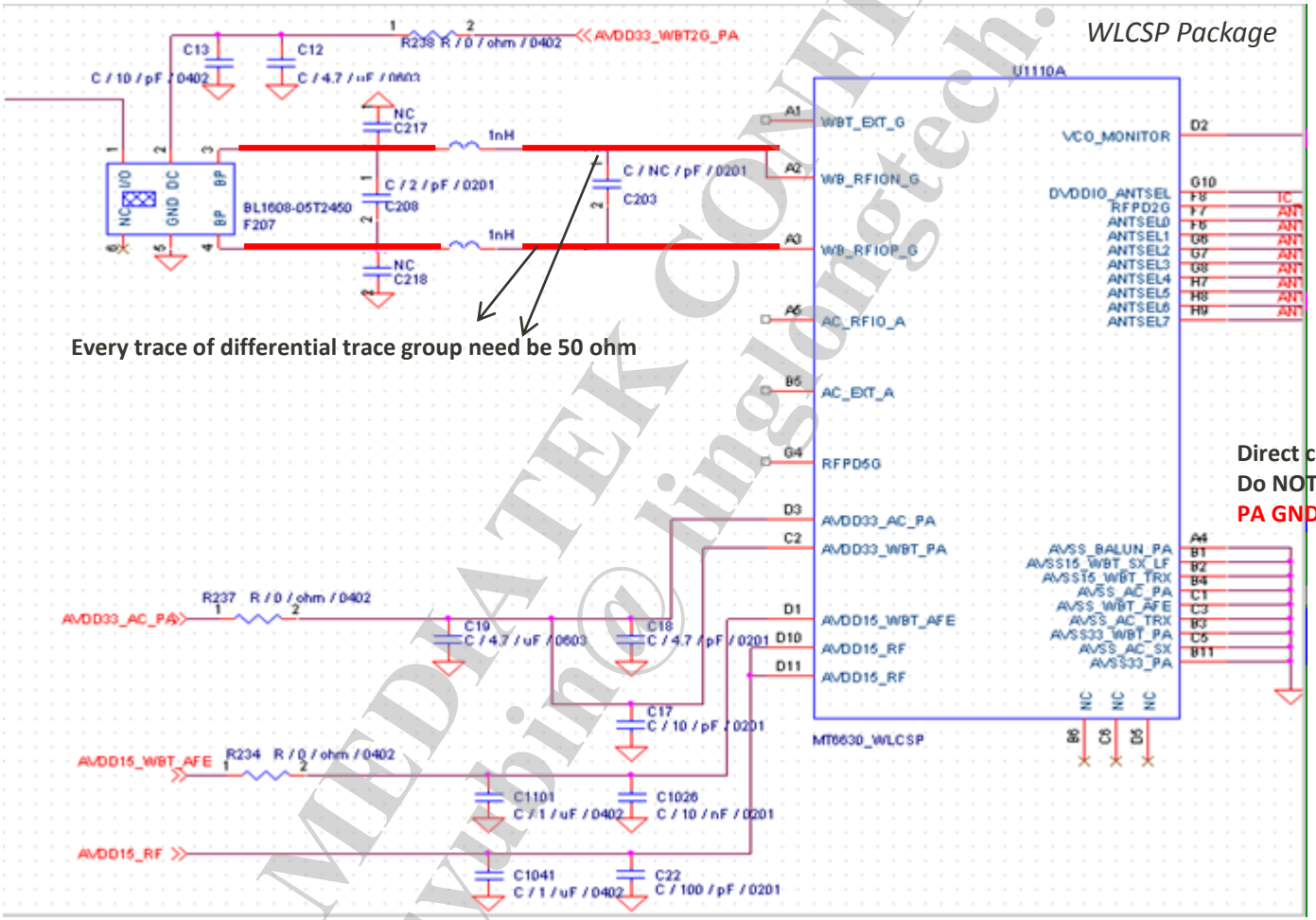
- **Bluetooth features**
  - Supported Bluetooth 4.1+HS, BT Low Energy (LE)
  - Bluetooth specification 3.0+HS compliance
  - High TX output power and good RX sensitivity
  - The good DEVM performance at high TX output power
  - Support ANT/ANT+ (Sharing the BT GFSK HW structure)
  - Support LPS(Low Power Scan)
  - Support LTE co-existence

Bluetooth	Test @ balun in/out			
Item	Condition	MT6630 T	MT6628	Unit
Rx sensitivity	BDR	-95	-95	dBm
Rx sensitivity	2EDR	-95	-94	dBm
Rx sensitivity	3EDR	-89	-87	dBm
Rx sensitivity	BLE	-98	-96	dBm
Tx power	BDR	12	10	dBm
Tx power	2EDR	9	7	dBm
Tx power	3EDR	9	7	dBm
Tx power	BLE	4	3	dBm

BT			
Item	Condition(VBAT=3.8V)	MT6630 T	Unit
BT Rx current	3DH5 Rx level : -88dBm	29	mA
BT Rx current	DH5 Rx level : -95dBm	29	mA
BT Tx current	3DH5 Tx level : 9.6dBm	60.5	mA
BT Tx current	DH5 Tx level :12.5dBm	73	mA
Sleep current	Sleep (Vcore= 1.2V)	0.12	mA
BLE scenario current	300ms periodic passive scan ; 11.25ms Rx scan window	1.5	mA
BLE scenario current	1280ms (3 Tx + 3 Rx) Undirected connectable advertise /ADV_IND	0.2	mA
BLE scenario current	500ms (3 Tx + 3 Rx) Undirected connectable advertise /ADV_IND	0.34	mA
BLE scenario current	1280 ms connection interval (MASTER) (1T + 1R)	0.17	mA
BLE scenario current	1280 ms connection interval (SLAVE) (1R + 1T)	0.2	mA

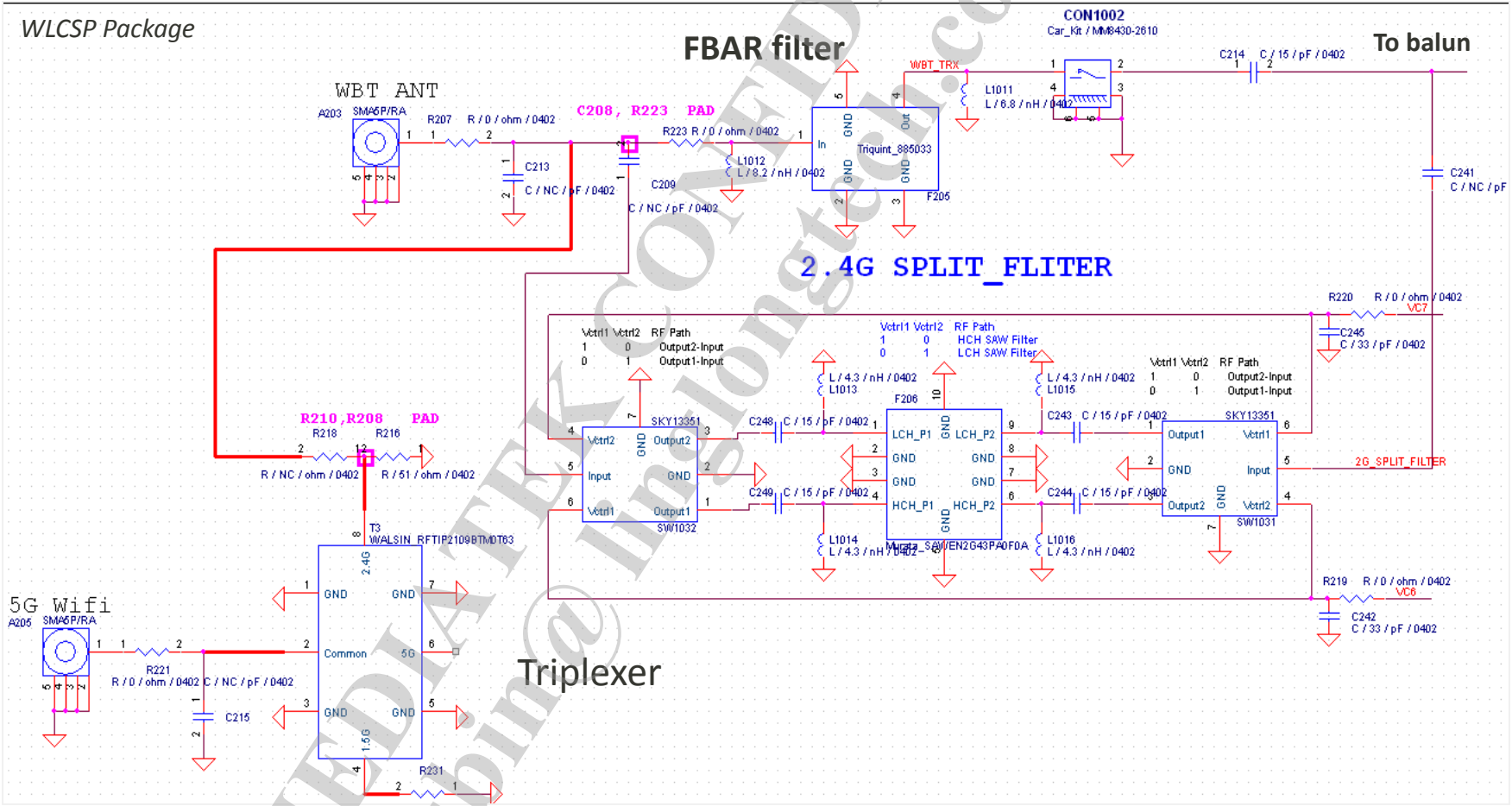
BT Application Circuit (WLCSP)

- RF differential-end trace (A2,A3 to Balun Pin3&Pin4)need to keep equal length and have solid ground plane
- Make star connection for AVDD15_RF(D10,D11)，also make star connection for AVDD33_PA(D3,C2)
- All the decoupling capacitors need be close to the power pin(balun Pin2,chip D10,D11,C2,D1,D3)
- Keep AVDD15_RF, AVDD15_WBT_AFE away from noisy traces e.g. PALDO 3.3V, SDIO bus, switching power supply, clock, and antenna control signals
- All the GND need be connected to the main GND directly (using VIAs)



BT Front–End structure (WLCSP)

- We has two choices for BT front End structure， one is FBAR filter， the other is using spilter filter
- Spilter filter configration supports the better LTE-coexistence performance
- We can share WIFI ANT using a Triplexer to receive the BT signal



All the RF trace need be designed to 50 Ohm @working frequency

BT audio interface for Dual talk

- WLCSP has two sets of PCM bus ,one of them is multiplexed from I2S bus
- QFN also has two sets of PCM bus , one of them is multiplexed from UART bus

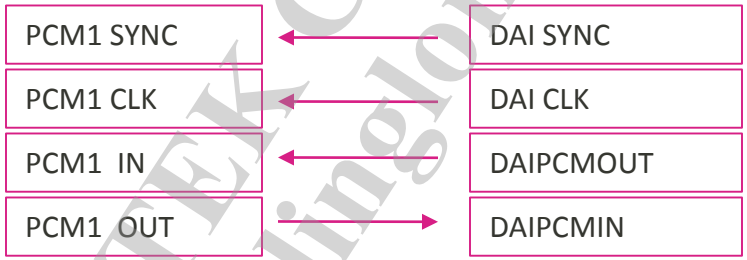
WLCSP Package

I2S_CLK	PCM2_CLK
I2S_WS	PCM2_SYNC
I2S_DATA_OUT	PCM2_IN
I2S_DATA_IN	PCM2_OUT

QFN Package

WIFI_INT_B(W) / GPIO0(Q)	PCM2_OUT
UART_RX	PCM2_CLK
UART_TX	PCM2_SYNC
UART_CTS	PCM2_IN

Default PCM1 bus connection to the Host AP



CONFIDENTIAL B

MT6630T FM Part Design Notice

Version : V03

MT6630T FM Rx Feature and Performance

- FM features and performance
  - FM 65-108MHz band with 50kHz step and RDS/RBDS supported
  - Audio sensitivity 3dBμVemf at (SINAD=26dB)
  - RDS sensitivity 18dBμVemf at RDS Dev.=2kHz， 5% BLER
  - Digital audio interface (I2S)

FM Rx Performance				
Item	Condition	MT6628	MT6630T	Unit
SINAD	Mono 22.5kHz	60	62	dB
Sensitivity	SINAD = 26dB	2	2~3	dBuVemf
THD	dev : 75KHz	0.05	0.05	%
ACI	@ -200KHz	55	55	dB
ACI	@ -400KHz	70	68	dB
Stereo separation ratio	Stereo 22.5kHz	40	50	dB
AM Suppression		62	58	dB

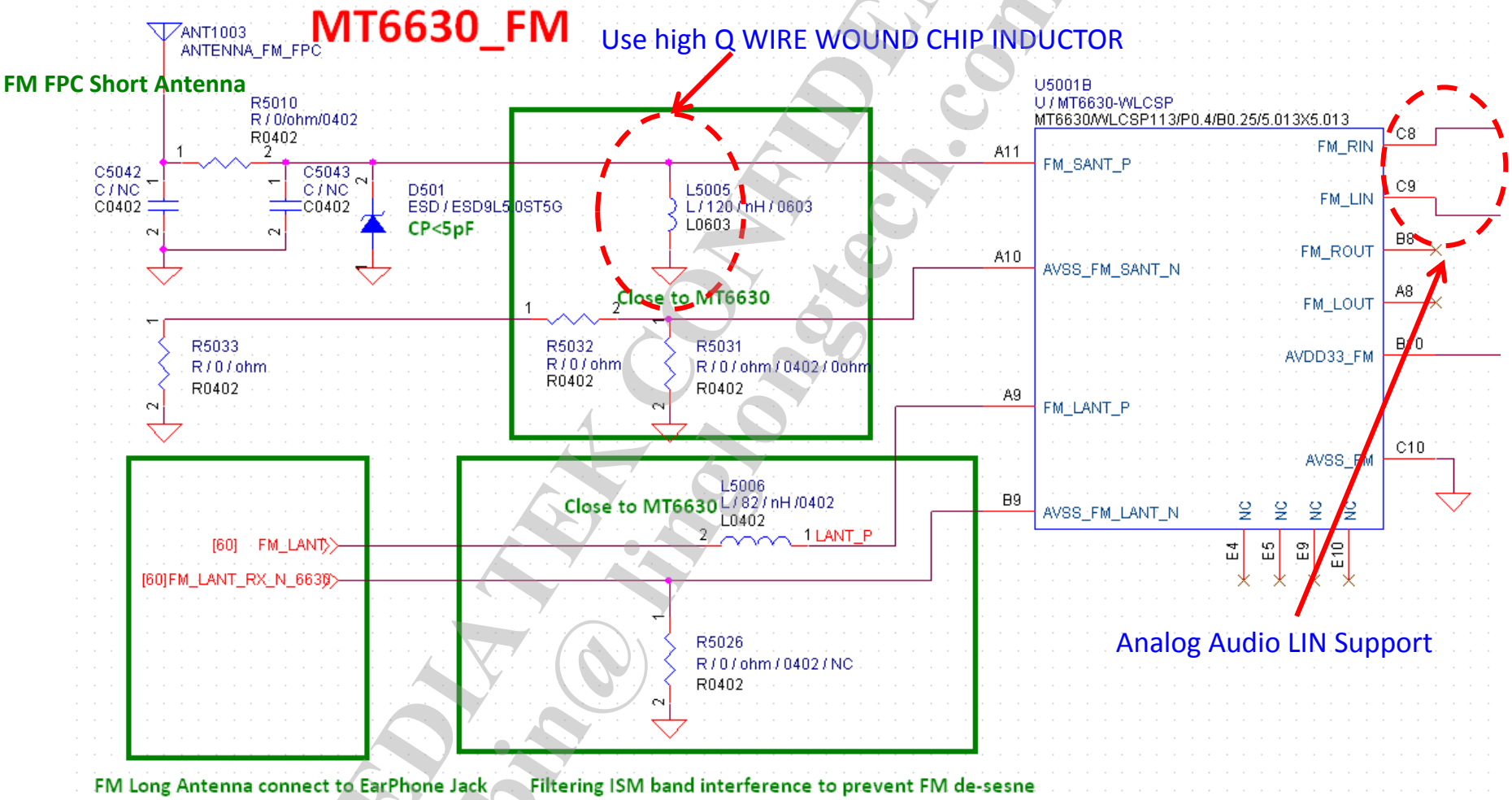
MT6630T FM Transmitter Feature and Performance

- FM features and performance
  - FM 65-108MHz band with 50KHz step / Supports RDS/RBDS encode
  - Supports digital audio input (I2S)
  - Programmable audio line in (maximum 1.4Vpk)
  - Audio Control：
    - Dynamic Range Control
    - Audio Limiter inside
    - Pre-emphasis
    - Programmable stereophonic MPX
  - Programmable deviation
  - Max output power range =13dBm

FM			
Item	Condition	Number	Unit
TX Power accuracy	Stereo 68.25k/Pre-emphasis 75us/pilot 6.75k	± 2	dB
Deviation accuracy	Stereo 68.25k/Pre-emphasis 75us/pilot 6.75k	± 5	%
Audio Stereo Separation	Stereo 68.25k/Pre-emphasis 75us/pilot 6.75k	40	dB
Audio SNR	Stereo 68.25k/Pre-emphasis 75us/pilot 6.75k	60	dB
Audio THD	Stereo 68.25k/Pre-emphasis 75us/pilot 6.75k	0.1	%

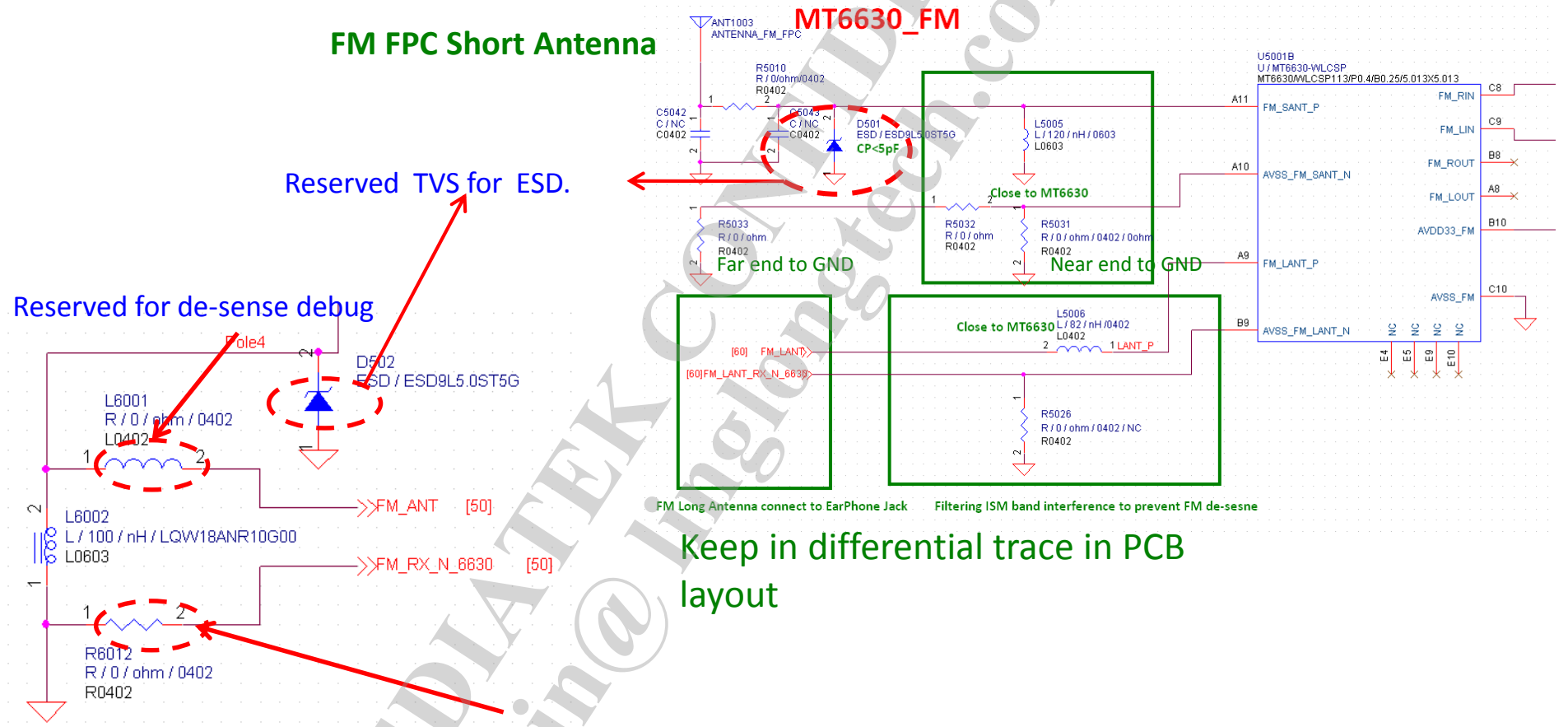
MT6630T FM TX Application Circuit

- Reserve matching network for short-ant
- Use high Q WIRE WOUND CHIP INDUCTOR for FM short-ant



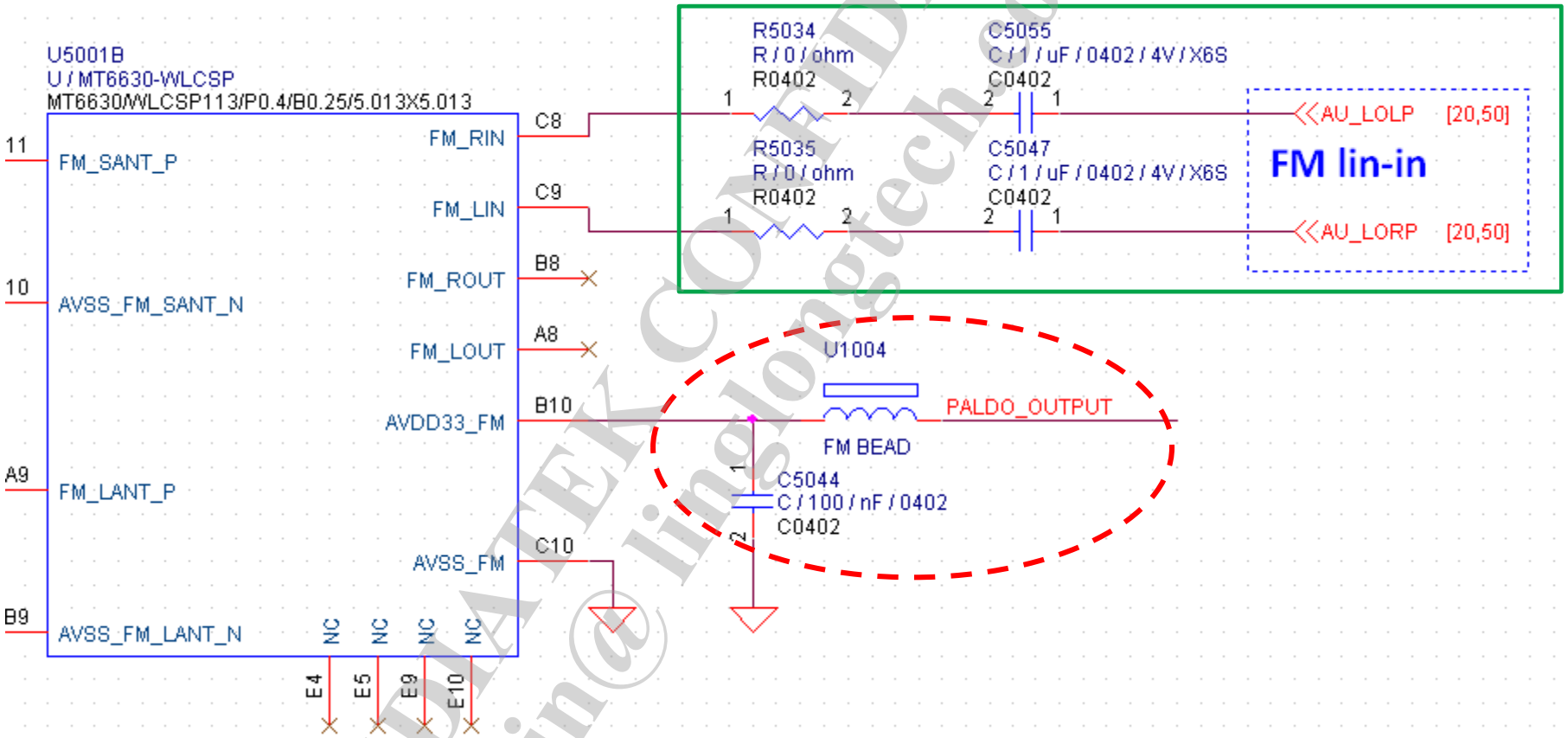
MT6630T FM RX Application Circuit (1/2)

- **Keep the FM_RX_N and FM_RX_P (LANT/SANT) in differential trace to connect with audio jack or FTP.**
- **Keep FM Antenna RF path away from power source.**



MT6630T FM RX Application Circuit (2/2)

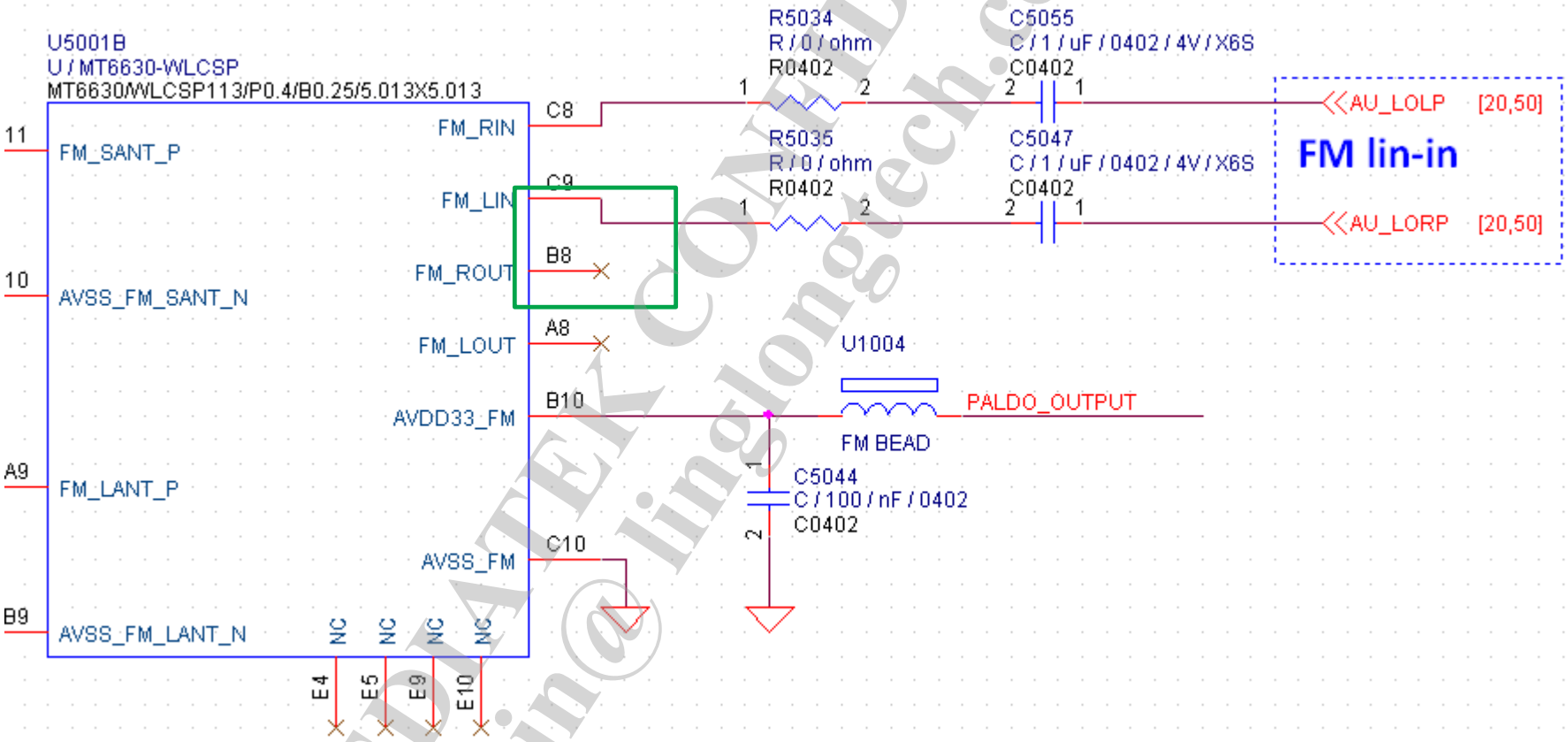
- Place de-coupling caps C5044 as close as possible to MT6630T .
- Reserve FM bead (ex.600ohm at 100MHz) at AVDD33_FM.



MT6630T FM Audio Interface selection

FM audio interface selection

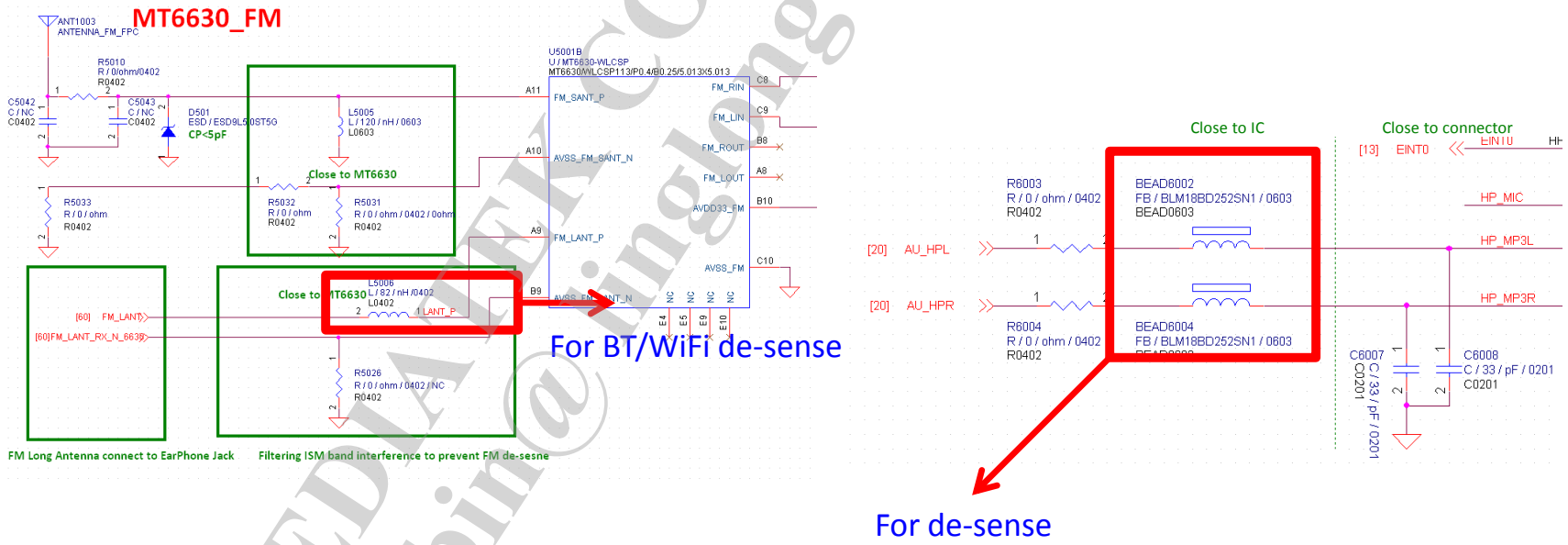
- **Analog Audio interface LOUT**
- **Digital Audio interface I2S**



MT6630T FM De-sense Note

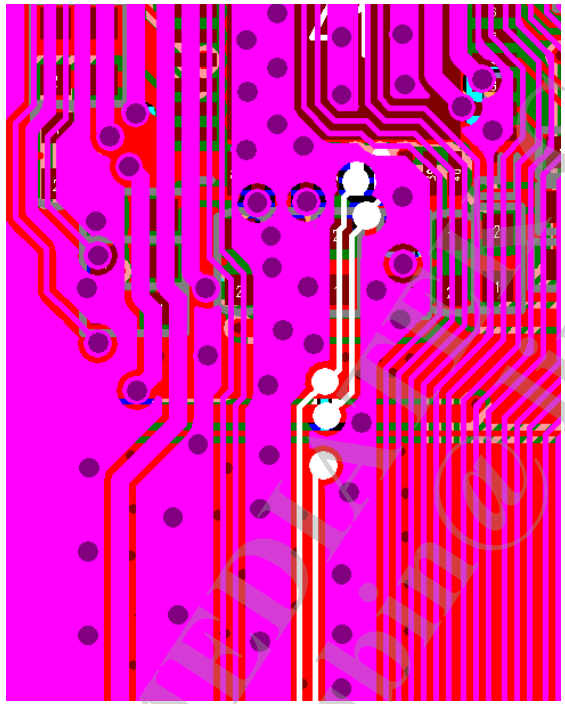
- Add 82nH on FM long Antenna trace, for WLAN/BT out band blocking de-sense.
- Keep FM Antenna(audio jack/ usb/FPC) and RF traces away from power source and other Antenna like WLAN/BT/GSM Antenna, to avoid de-sense.
- RF Traces should be far away and well- grounded from Vbat / VDDK and any other VDD traces.
- VFM trace should be well ground shielding.
- MP3_OUTL/R close to chip should add beads for de-sense.

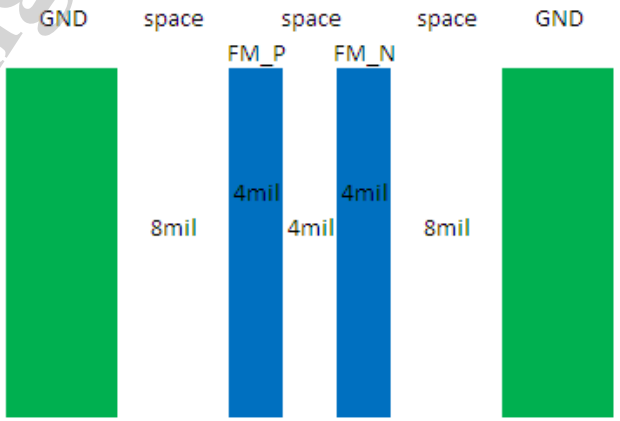
FM FPC Short Antenna



FM RF trace PCB layout

- PCB trace should be differential and as balanced as possible, for immunity to common mode noise.
- The distance from FM RF trace to Audio-Jack is generally long, Please MUST routed as 1st priority in the beginning arrangement stage, and shielded completely by ground. Bad protection for FM may cause fake station or noise issue.
- Also, route FM trace in inner layer with ground shield to prevent ESD event.





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