everyday genius

MT8516A Application Processor
Technical Brief

Version: 0.91
Release date: 2017-12-08

Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
0.1	2016-10-05	Lifang Wang	Initial draft
0.2	2017-02-28	Lifang Wang	Added Package details table to Package Information section. DDR parameter requirements at component pin DDR3 skew tolerances Added Parameter Specifications for I2C, eMMC, SD. Remove analog IP operation temperature info. Add digital IO type specifications Add more description of WiFi/BT RF radio Update WiFi/BT BLE transmitter specifications Update XO component spec requirement Updated Audio Downlink/Uplink Block Diagrams
0.2	2017-03-08	Lifang Wang	Update Table 2-23: DDR parameter requirements at component pin Add Figure 2-14. Control Overshoot and Undershoot Definition Block
0.2	2017-03-10	Lifang Wang	Remove the CSI Character Modify the 2.1.4 interface Application Notice table
0.2	2017-03-15	Lifang Wang	Update Table 2-44: Basic data rate receiver specification Update Table 2-48 Bluetooth LE receiver specification Update Table 2-49 Bluetooth LE transmitter specification
0.3	2017-03-30	Lifang Wang	Table 2-41: update the parameter
0.3	2017-04-20	Lifang Wang	Modified WiFi/BT RF Table 2-42~Table 2-49 specification tables again. Update Table 2-56. Package Details.
0.4	2017-08-17	Lifang Wang	Table 2-41: add unit Add DMIC Capability
0.4	2017-08-22	Lifang Wang	Table 2-41: update parameter
0.4	2017-08-30	Lifang Wang	Update document's format
0.5	2017-09-09	Lifang Wang	Update the document's format and 2.7.1 Reference Clock, delete table for Reference clock operation mode
0.6	2017-09-19	Lifang Wang	Fix table type error, for DAC change is in table 2-41
0.7	2017-11-05	Lifang Wang	Modify Table 2-1 ball name WBT_EXT_G & GPS_DPX_RFOUT to NC. Table 0-1 WBT_EXT_G & GPS_DPX_RFOUT is NC ball, remove the description. Fix type error MLD4→ NLD4, APK→ SPK. Table 2-15: change the pin name to function is not match. Table 0-2: remove function which is not match.

0.8	2017-11-26	Lifang Wang	Restore the pin rename for MIPI, HDMI, Camera to avoid confuse. Update Figure 0-1 and table 2-15.
0.9	2017-11-30	Lifang Wang	Modify table 2-45, BT LT receiver Out-of-band blocking max parameter to min
0.91	2017-12-08	Lifang Wang	Fix some table missing

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Lists of Tables and Figures

1 System Overview

MT8516A is a highly integrated connected audio platform incorporating application processing and connectivity subsystems designed to enable connected audio applications. The chip integrates a Quad-core ARM® Cortex-A35 MPCore™ operating up to 1.3 GHz. The MT8516A interfaces to NAND flash memory, LPDDR2, LPDDR3, DDR3, DDR3L and DDR4 for optimal performance and also supports booting from eMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces such as TDM/PDM inputs are included for microphone voice input control / search applications on connected audio products.

The application processor, a Quad-core ARM® Cortex-A35 MPCore™, includes a NEON multimedia processing engine.

MT8516A includes two wireless connectivity functions: WLAN and Bluetooth. These built-in RF parts of those two block scans support 802.11 b/g/n. With two advanced radio technologies integrated into a single chip, MT8516A provides the industry's best and most convenient connectivity solution. MT8516A implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It also supports single antenna sharing among 2.4 GHz antenna for Bluetooth, WLAN. The enhanced overall quality is achieved for simultaneous voice, data, and audio transmission. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Platform Features

- **AP MCU subsystem**
  - Quad-core ARM® Cortex-A35 MPCore™ operating at 1.3 GHz
  - NEON multimedia processing engine with SIMDv2 / VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 1.05V to 1.31V

- **Wireless Connectivity MCU subsystem**
  - Andes N9 processor with 48KB I-cache, 40KB D-cache

- **External memory interface**
  - Supports LPDDR2, LPDDR3, DDR3/L, DDR4 up to 2GB
  - 32-bit data bus width
  - Memory clock up to 800 MHz
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control

- **Security**
  - ARM® TrustZone® Security

- **Storage**
  - NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
  - 3 sets of memory card controller supporting SD/SDHC/MMC and SDIO2.0/3.0 protocols

- **Connectivity**
  - Two USB ports, port0 support USB 2.0 OTG mode but port1 only support USB 2.0 host mode. The two USB20 ports support connection Hub to transfer data communications with HS/FS/LS Device. USB2.0 high-speed dual mode supporting 8 Tx and 8 Rx endpoints.
  - 3 UARTs for external devices and debugging interfaces
  - SPI master for external devices
  - 3 I2C to control peripheral devices, e.g. CMOS image sensor, or LCM module
  - I2S master output and master/slave input for connection with optional external hi-end audio codec
  - GPIOs
  - 10M/100M Ethernet MAC with MII and RMII interface
  - IR receiver

- **Operating conditions**
  - Core voltage: 1.15V
  - Processor DVFS+SRAM voltage : 1.15V~1.31V (Typ. 1.15V ; sleep mode 0.85V)
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V/1.35V/1.5V
  - NAND: 1.8V/3.3V
  - LCM interface: 1.8V/3.3V
  - Clock source: 26-MHz, 32.768-kHz

- **Package**
  - Type: WB TFBGA
  - 12.6mm x 13.1mm
  - Height: 1.2 mm maximum
  - Ball count: 406 balls
  - Ball pitch: 0.5mm

1.2 Multimedia Features

- **Audio**
  - I2S Master Mode sampling rates supported: 8kHz to 192kHz
  - I2S In Slave mode sampling rates supported: 8kHz to 48kHz
  - Sample formats supported: 16-bit/24-bit, Mono/Stereo
  - Interfaces supported: DAI, I2S, TDM, SPDIF
  - Flexible and powerful audio post-processing technologies
  - Supports DIR(SPDIF-input) decode: supports 32, 44.1, 48, 88.2, 96kHz sample rate.
  - Supports SPDIF-output encode: supports 32, 44.1, 48, 88.2, 96kHz sample rate.
  - Supports Time Division Multiplexer I2S output (master mode only): supports 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 192kHz sample rate and channel number up to 2/4/8 in configuration by 1/2/4 data pins (corresponding to 2/4/8 channels),
  - Dedicated pin for TDM TX (not share clock pins with TDM RX).
  - Supports Time Division Multiplexer input: supports 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 192kHz sample rate and channel number up to 2/4/8 in 1 serial data pin,
  - Dedicated pin for TDM RX (not share clock pins with TDM TX).
- **Speech**
  - Noise reduction
  - Noise suppression
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC input
  - Digital MIC input

1.3 Wi-Fi/Bluetooth Features

- **Supports integrated Wi-Fi/Bluetooth**
  - Supports single antenna for Bluetooth and WLAN
  - Self calibration
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (for example, transmit window and duration that take into account protocol exchange sequence, frequency, etc.)

- **Wi-Fi**
  - Single-band (2.4GHz) single stream 802.11 b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (Hardware)
  - QoS: WFA WMM, WMM PS
  - Supports 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard)
  - Supports HotSpot 2.0 Passpoint
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth v4.0 Low Energy (LE)
  - Rx sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality
  - Low-power scan function to reduce power consumption in scan modes

1.4 General Description

The MediaTek MT8516A has integrated 802.11 b/g/n and Bluetooth 4.0 + HS radios and passive devices (IPD) to provide a connected audio solution. The application processor incorporates a high efficient 64-bit Quad Cortex-A35 processor operating at 1.3 GHz. Rich memory interfaces (PCDDR3, DDR4, LPDDR3, eMMC, Raw NAND) provide high flexibility to support variant memory configurations. The elaborate MMD (MediaTek Module Design) provides verified schematics and PCB layout for memory and power source to reduce development time. Combo chip MT6630, 802.11ac/BT also gives the alternative to fulfill high end Wi-Fi/BT requirement. The MT8516A processor delivers high-performance computing, low-power consumption, and good multimedia experience.

World-leading technology

Based on MediaTek's world-leading SoC architecture with advanced 28nm RF process, the MT8516A integrates digital and RF into a single chip that is suitable for compact PCB design. The PMIC MT6392 is designed to supply all the power to MT8516A itself. The two-chip solution brings lower rBOM and design effort to cost-effectively develop applications with fast time to market.

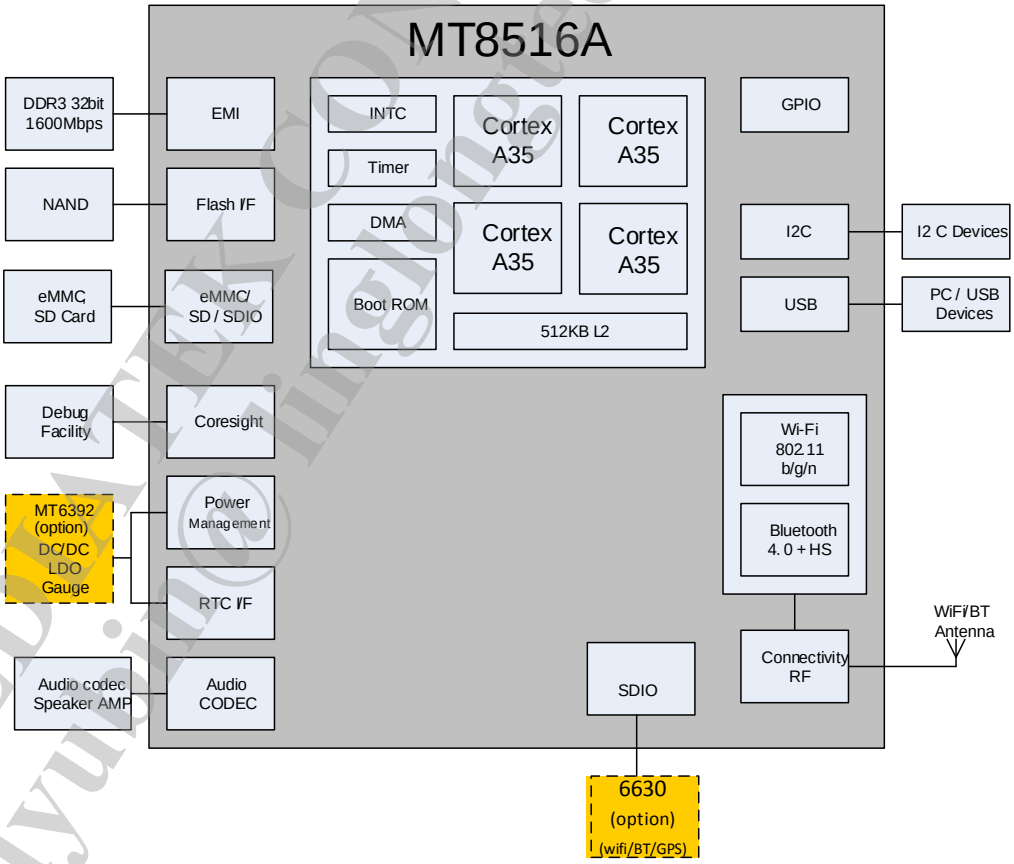


Figure 1-1: MT8516A Block Diagram

2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

406	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	GNDK	GNDK	ED1	ED5	ED4		ED13	ED11	ECKE		EA1		EA5	EA9	ECS0	ERAS	EBA2		ED30	ED7	ED21	ED20	ED18	GNDK	GNDK	A
B		ED10	ED14	ED3	ED7	ED2	ED15		EA10	EA8	EA4	EBA1	EA3	EA13	ERWE	ECAS	ECS1	ED24	ED26	ED28	ED19	ED22	ED16	ED31		B
C	REXTDN		ED8	ED12	ED6	ED0	ED9	EDQM1		EA14	EA6	EA0	VCCIO		VCCIO	EPRESET			EDQM2		EDQS2	ED23	ED23	ED25	ED27	C
D	MSDC1_CLK	MSDC1_DAT0	MSDC1_DAT1				EDQS1		EDQS0		ECLK0_B	EA7			EBA0	ECLK1			EDQS3		EDQS2_B		MSDC0_DAT7	MSDC0_DAT5	MSDC0_DAT6	D
E		MSDC1_DAT3	MSDC1_CMD		EDQM0		EDQS1_B		EDQS0_B		ECLK0	EA12			EA2	ECLK1_B			EDQS3_B		EDQM3		MSDC0_DAT4	MSDC0_DAT3		E
F	DVDD28_MSDC1	MSDC1_DAT2			AVDD18_MEMP		GNDK	GNDK	GNDK			EA11			EA15	GNDK	GNDK	GNDK		GNDK	GNDK		MSDC0_DAT2	MSDC0_DAT0	MSDC0_DAT1	F
G	AVDD18_MIPIRX		CMDAT0	CMDAT1	DVDD18_IO0	CMMCLK	CMPCLK	RTN	RTP	VCCIO		VCCIO			VCCIO		VCCIO			GNDK	GNDK	MSDC0_CMD	MSDC0_CLK	MSDC0_RSTB	DVDD28_MSDC	G
H	RDN0_A	RDP0_A	GNDK							GNDK	GNDK							GNDK		GNDK				EINT14	DVDD28_NFI	H
J		RDN1_A	RDP1_A	RCP_A	RCN_A	GNDK	GNDK		GNDK	VCCK		GNDK			GNDK			VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC		EINT17	EINT16		J
K	RDN0	RDP0						DVDD18_EFUSE	FSOURCE_P	VCCK	GNDK	GNDK	GNDK	VCCK		VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC	VCCK_VPROC		EINT22	EINT21	EINT15	K
L		RDN1	RDP1						VCCK						VCCK_VPROC								PWRAP_SPI0_CSN	PWRAP_SPI0_MO	EINT23	L
M	AVDD18_MIPITX	RDN2	RDP2	RCN	RCP	AVSS18_MIPI			VCCK			GNDK	GNDK			VCCK_VPROC		CLKO_32K		RTC32K_CK	SDA2	SCL2	PWRAP_SPI0_	PWRAP_SPI0_		M
N		RDN3	RDP3	TCP	TCN	AVSS18_MIPI			VCCK	VCCK	GNDK	GNDK	GNDK	GNDK				AVSS22_XO_32		AVDD22_XO_32		SYSRSTB	SRCLKENA	PWRAP_INT	DVDD18_IO3	N
P	VRT	TDP0	TDN0				GNDK		VCCK			GNDK	GNDK	GNDK	GNDK	VCCK_VPROC		GNDK						WATCHDOG		P
R		TDP1	TDN1						VCCK	VCCK	GNDK	GNDK	GNDK	GNDK							AU_LOLP				AVDD28_AUDIO	R
T	TDP2	TDN2		TDP3	TDN3	AVSS18_MIPI			GNDK		GNDK	GNDK	GNDK	GNDK	VCCK		AU_TN		AU_HPR	AU_HPL	AU_LOLN		AVSS_AUDIO	AU_VIN0_N	AU_VIN0_P	T
U			DSI_TE	DVDD18_IO1	LCM_RST	DISP_PWM	SCL0	SDA0	GNDK		VCCK	VCCK	GNDK				AU_TP						AU_VIN2_N	AU_VIN2_P		U
V	JTDO	JTDI	JTMS												VCCK	VCCK	GNDK	AUX_IN2	AUX_IN4	AUX_IN0	AUX_IN1		AU_VIN1_N	AU_VIN1_P	AVDD22_AUDIO	V
W	TESTMODE	SCL1	JTCK		AVDD18_WBT_AFE	AVDD18_WBT		NC		GNDK				GNDK	GNDK			GNDK	AVDD18_HDMITX	AUX_IN3	AUX_IN5	AVDD18_PLLGP	ACCDET	AU_MICBIAS1	AU_MICBIAS0	W
Y		SDA1	KPCOL1	AVSS_CONN	AVSS_CONN	AVSS_CONN	AVSS_CONN		AVSS_CONN	AVSS_CONN	MSDC2_CLK			EINT6	EINT11			AVDD33_USB						AVSS18_AP	AVDD18_AP	Y
AA	KPROW1	KPCOL0	KPROW0	AVSS_CONN	AVSS_CONN	AVSS_CONN	AVSS_CONN	AVSS_CONN	AVSS_CONN	AVSS_CONN	MSDC2_CMD			EINT1	EINT8			CHD_DM_P0					CLKO_26M	AVSS18_PLLGP	REFP	AA
AB	UTXD1	URXD1	AVSS_CONN	AVSS_CONN	AVSS_CONN	AVSS_CONN	AVSS_CONN	AVSS_CONN		AVSS_CONN	MSDC2_DAT3			EINT5	EINT13			CHD_DP_P0			HDMITX_CLK_P		AVDD22_XO		AVSS22_XO	AB
AC	UTXD0	URXD0		AVSS_CONN	AVSS_CONN			EINT18		SPI_CS	MSDC2_DAT2			EINT0	EINT2			USB_VRT_P0			HDMITX_CLK_M	HDMITX_CH0_P			XO_IN	AC
AD	I2S_LRCK	I2S_BCK	AVSS_CONN	WB_RFIN	NC	AVDD33_WBT	EINT19	HDMISD	SPI_CK	SPI_MO		EINT3	EINT4	EINT10	EINT3	MRG_DO			USB_DM_P1	USB_DM_P0		HDMITX_CH0_M	HDMITX_CH1_P	HDMITX_CH2_P	AVSS22_XO	AD
AE	DUMMY	I2S_DATA_IN	AVSS_CONN				EINT20	CEC	HDMISCK	SPI_MI	MSDC2_DAT1	EINT12	EINT24	EINT25	URXD2	UTXD2	MRG_CLK	AVSS33_USB	USB_DP_P1	USB_DP_P0	AVSS18_HDMIT		HDMITX_CH1_M	HDMITX_CH2_M	DUMMY	AE
AF	DUMMY	DUMMY	AVSS_CONN					HTPLG	DVDD18_IO2		MSDC2_DAT0	DVDD28_MSDC		EINT7	DVDD28_DPI		MRG_SYNC	MRG_DI	AVDD18_USB		USB_VBUS_P0	HDMITX_REXT			DUMMY	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Figure 2-1: DDR3 (2*16bits) ball map view of MT8516A

2.1.2 Pin Coordinate

Table 2-1: DDR3 (2*16bits) Pin Coordinates

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
A1	GNDK	J6	GNDK	W1	TESTMODE
A2	GNDK	J7	GNDK	W2	SCL1
A3	ED1	J9	GNDK	W3	JTCK
A4	ED5	J10	VCCK	W5	AVDD18_WBT_AFE
A5	ED4	J12	GNDK	W6	AVDD18_WBT
A7	ED13	J15	GNDK	W8	NC
A8	ED11	J18	VCCK_VPROC	W10	GNDK
A9	ECKE	J19	VCCK_VPROC	W14	GNDK
A11	EA1	J20	VCCK_VPROC	W15	GNDK
A13	EA5	J21	VCCK_VPROC	W18	GNDK
A14	EA9	J23	EINT17	W19	AVDD18_ANA
A15	ECS0	J24	EINT16	W20	AUX_IN3
A16	ERAS	K1	RSV20	W21	AUX_IN5
A17	EBA2	K2	RSV21	W22	AVDD18_PLLGP
A19	ED30	K8	DVDD18_EFUSE	W23	ACCDET
A20	ED17	K9	FSOURCE_P	W24	AU_MICBIAS1
A21	ED21	K10	VCCK	W25	AU_MICBIAS0
A22	ED20	K11	GNDK	Y2	SDA1
A23	ED18	K12	GNDK	Y3	KPCOL1
A24	GNDK	K13	GNDK	Y4	AVSS_CONN
A25	GNDK	K14	VCCK	Y5	AVSS_CONN
B2	ED10	K16	VCCK_VPROC	Y6	AVSS_CONN
B3	ED14	K17	VCCK_VPROC	Y7	AVSS_CONN
B4	ED3	K18	VCCK_VPROC	Y9	AVSS_CONN
B5	ED7	K19	VCCK_VPROC	Y10	AVSS_CONN

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
B6	ED2	K20	VCCK_VPROC	Y11	MSDC2_CLK
B7	ED15	K21	VCCK_VPROC	Y14	EINT6
B9	EA10	K23	EINT22	Y15	EINT11
B10	EA8	K24	EINT21	Y18	AVDD33_USB
B11	EA4	K25	EINT15	Y24	AVSS18_AP
B12	EBA1	L2	RSV18	Y25	AVDD18_AP
B13	EA3	L3	RSV19	AA1	KPROW1
B14	EA13	L9	VCCK	AA2	KPCOL0
B15	ERWE	L15	VCCK_VPROC	AA3	KPROW0
B16	ECAS	L23	PWRAP_SPI0_CSN	AA4	AVSS_CONN
B17	ECS1	L24	PWRAP_SPI0_MO	AA5	AVSS_CONN
B18	ED24	L25	EINT23	AA6	AVSS_CONN
B19	ED26	M1	AVDD18_ANA	AA7	AVSS_CONN
B20	ED28	M2	RSV14	AA8	AVSS_CONN
B21	ED19	M3	RSV15	AA9	AVSS_CONN
B22	ED22	M4	RSV16	AA10	AVSS_CONN
B23	ED16	M5	RSV17	AA11	MSDC2_CMD
B24	ED31	M6	AVSS18_ANA	AA14	EINT1
C1	REXTDN	M9	VCCK	AA15	EINT8
C3	ED8	M12	GNDK	AA18	CHD_DM_P0
C4	ED12	M13	GNDK	AA23	CLKO_26M
C5	ED6	M16	VCCK_VPROC	AA24	AVSS18_PLLGP
C6	ED0	M18	CLKO_32K	AA25	REFP
C7	ED9	M20	RTC32K_CK	AB1	UTXD1
C8	EDQM1	M21	SDA2	AB2	URXD1
C10	EA14	M22	SCL2	AB3	AVSS_CONN
C11	EA6	M23	PWRAP_SPI0_CK	AB4	AVSS_CONN

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
C12	EA0	M24	PWRAP_SPI0_MI	AB5	AVSS_CONN
C13	VCCIO	N2	RSV12	AB6	AVSS_CONN
C15	VCCIO	N3	RSV13	AB7	AVSS_CONN
C16	ERESET	N4	RSV06	AB8	AVSS_CONN
C19	EDQM2	N5	RSV05	AB10	AVSS_CONN
C21	EDQS2	N6	AVSS18_ANA	AB11	MSDC2_DAT3
C22	ED23	N9	VCCK	AB14	EINT5
C23	ED29	N10	VCCK	AB15	EINT13
C24	ED25	N11	GNDK	AB18	CHD_DP_P0
C25	ED27	N12	GNDK	AB21	RSV41
D1	MSDC1_CLK	N13	GNDK	AB23	AVDD22_XO
D2	MSDC1_DAT0	N14	GNDK	AB25	AVSS22_XO
D3	MSDC1_DAT1	N18	AVSS22_XO_32K	AC1	UTXD0
D7	EDQS1	N20	AVDD22_XO_32K	AC2	URXD0
D9	EDQS0	N22	SYSRSTB	AC4	AVSS_CONN
D11	ECLK0_B	N23	SRCLKENA	AC5	AVSS_CONN
D12	EA7	N24	PWRAP_INT	AC8	EINT18
D15	EBA0	N25	DVDD18_IO3	AC10	SPI_CS
D16	ECLK1	P1	RSV11	AC11	MSDC2_DAT2
D19	EDQS3	P2	RSV10	AC14	EINT0
D21	EDQS2_B	P3	RSV09	AC15	EINT2
D23	MSDC0_DAT7	P7	GNDK	AC18	USB_VRT_P0
D24	MSDC0_DAT5	P9	VCCK	AC21	RSV40
D25	MSDC0_DAT6	P12	GNDK	AC22	RSV43
E2	MSDC1_DAT3	P13	GNDK	AC25	XO_IN
E3	MSDC1_CMD	P14	GNDK	AD1	I2S_LRCK
E5	EDQM0	P15	GNDK	AD2	I2S_BCK

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
E7	EDQS1_B	P16	VCCK_VPROC	AD3	AVSS_CONN
E9	EDQS0_B	P18	GNDK	AD4	WB_RFIN
E11	ECLK0	P24	WATCHDOG	AD5	NC
E12	EA12	R2	RSV08	AD6	AVDD33_WBT
E15	EA2	R3	RSV07	AD7	EINT19
E16	ECLK1_B	R9	VCCK	AD8	RSV38
E19	EDQS3_B	R10	VCCK	AD9	SPI_CK
E21	EDQM3	R11	GNDK	AD10	SPI_MO
E23	MSDC0_DAT4	R12	GNDK	AD12	EINT9
E24	MSDC0_DAT3	R13	GNDK	AD13	EINT4
F1	DVDD28_MSDC1	R14	GNDK	AD14	EINT10
F2	MSDC1_DAT2	R21	AU_LOLP	AD15	EINT3
F5	AVDD18_MEMPLL	R25	AVDD28_AUDIO	AD16	MRG_DO
F7	GNDK	T1	RSV04	AD19	USB_DM_P1
F8	GNDK	T2	RSV03	AD20	USB_DM_P0
F9	GNDK	T4	RSV02	AD22	RSV42
F12	EA11	T5	RSV01	AD23	RSV45
F15	EA15	T6	AVSS18_ANA	AD24	RSV47
F16	GNDK	T9	GNDK	AD25	AVSS22_XO
F17	GNDK	T11	GNDK	AE1	DUMMY
F18	GNDK	T12	GNDK	AE2	I2S_DATA_IN
F20	GNDK	T13	GNDK	AE3	AVSS_CONN
F21	GNDK	T14	GNDK	AE7	EINT20
F23	MSDC0_DAT2	T15	VCCK	AE8	RSV35
F24	MSDC0_DAT0	T17	AU_TN	AE9	RSV37
F25	MSDC0_DAT1	T19	AU_HPR	AE10	SPI_MI
G1	AVDD18_ANA	T20	AU_HPL	AE11	MSDC2_DAT1

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
G3	RSV33	T21	AU_LOLN	AE12	EINT12
G4	RSV34	T23	AVSS_AUDIO	AE13	EINT24
G5	DVDD18_IO0	T24	AU_VIN0_N	AE14	EINT25
G6	RSV32	T25	AU_VIN0_P	AE15	URXD2
G7	RSV31	U3	RSV30	AE16	UTXD2
G8	RTN	U4	DVDD18_IO1	AE17	MRG_CLK
G9	RTP	U5	RSV29	AE18	AVSS33_USB
G10	VCCIO	U6	RSV28	AE19	USB_DP_P1
G12	VCCIO	U7	SCL0	AE20	USB_DP_P0
G15	VCCIO	U8	SDA0	AE21	AVSS18_ANA
G17	VCCIO	U9	GNDK	AE23	RSV44
G20	GNDK	U11	VCCK	AE24	RSV46
G21	GNDK	U12	VCCK	AE25	DUMMY
G22	MSDC0_CMD	U13	GNDK	AF1	DUMMY
G23	MSDC0_CLK	U17	AU_TP	AF2	DUMMY
G24	MSDC0_RSTB	U23	AU_VIN2_N	AF3	AVSS_CONN
G25	DVDD28_MSDC0	U24	AU_VIN2_P	AF8	RSV36
H1	RSV26	V1	JTDO	AF9	DVDD18_IO2
H2	RSV27	V2	JTDI	AF11	MSDC2_DAT0
H3	GNDK	V3	JTMS	AF12	DVDD28_MSDC2
H10	GNDK	V15	VCCK	AF14	EINT7
H11	GNDK	V16	VCCK	AF15	DVDD28_MII
H18	GNDK	V17	GNDK	AF17	MRG_SYNC
H20	GNDK	V18	AUX_IN2	AF18	MRG_DI
H24	EINT14	V19	AUX_IN4	AF19	AVDD18_USB
H25	DVDD28_NFI	V20	AUX_IN0	AF21	USB_VBUS_P0
J2	RSV22	V21	AUX_IN1	AF22	RSV39

Ball Loc.	Ball name	Ball Loc.	Ball Name	Ball Loc.	Ball name
J3	RSV23	V23	AU_VIN1_N	AF25	DUMMY
J4	RSV25	V24	AU_VIN1_P		
J5	RSV24	V25	AVDD22_AUDIO		

Table 2-2: DDR Pinmux Table

PKG/PCB Ball Location	Pin-Mux 1 - PCDDR3 16bitx2	Pin-Mux 2 - PCDDR4 16bitx2	Pin-Mux 3 - LP3_DSC	Pin-Mux 4 - LP3_POP	Pin-Mux 5 - DDR3_X8
C23	ED29	ED30	ED15	ED24	ED28
C25	ED27	ED26	ED11	ED31	ED26
B24	ED31	ED24	ED14	ED29	ED30
C24	ED25	ED28	ED10	ED28	ED24
B20	ED28	ED27	ED13	ED11	ED23
A19	ED30	ED29	ED12	ED9	ED17
B19	ED26	ED25	ED8	ED13	ED21
B18	ED24	ED31	ED9	ED10	ED19
E21	EDQM3	EDQM3	EDQM1	EDQM3	EDQM3
D19	EDQS3	EDQS3	EDQS1	EDQS3	EDQS3
E19	EDQS3_B	EDQS3_B	EDQS1_B	EDQS3_B	EDQS3_B
A22	ED20	ED22	ED26	ED27	ED27
B23	ED16	ED16	ED31	ED26	ED31
A23	ED18	ED20	ED27	ED25	ED25
B22	ED22	ED18	ED30	ED30	ED29
B21	ED19	ED19	ED28	ED14	ED22
C22	ED23	ED21	ED29	ED12	ED18
A21	ED21	ED23	ED25	ED8	ED16
A20	ED17	ED17	ED24	ED15	ED20
C19	EDQM2	EDQM2	EDQM3	EDQM1	EDQM2
C21	EDQS2	EDQS2	EDQS3	EDQS1	EDQS2
D21	EDQS2_B	EDQS2_B	EDQS3_B	EDQS1_B	EDQS2_B
A08	ED11	ED12	ED7	ED5	ED12
B07	ED15	ED14	ED3	ED6	ED8
A07	ED13	ED8	ED2	ED7	ED10
C07	ED9	ED10	ED6	ED4	ED14
C03	ED8	ED13	ED5	ED19	ED3
C04	ED12	ED15	ED0	ED23	ED7
B02	ED10	ED9	ED4	ED17	ED5
B03	ED14	ED11	ED1	ED16	ED1
C08	EDQM1	EDQM1	EDQM0	EDQM0	EDQM1
D07	EDQS1	EDQS1	EDQS0	EDQS0	EDQS1
E07	EDQS1_B	EDQS1_B	EDQS0_B	EDQS0_B	EDQS1_B
C05	ED6	ED6	ED22	ED3	ED13
A05	ED4	ED4	ED18	ED1	ED11
C06	ED0	ED0	ED23	ED0	ED15
B06	ED2	ED2	ED19	ED2	ED9

PKG/PCB Ball Location	Pin-Mux 1 - PCDDR3 16bitx2	Pin-Mux 2 - PCDDR4 16bitx2	Pin-Mux 3 - LP3_DSC	Pin-Mux 4 - LP3_POP	Pin-Mux 5 - DDR3_X8
B05	ED7	ED7	ED21	ED20	ED4
A04	ED5	ED3	ED17	ED21	ED6
B04	ED3	ED5	ED20	ED18	ED2
A03	ED1	ED1	ED16	ED22	ED0
E05	EDQM0	EDQM0	EDQM2	EDQM2	EDQM0
D09	EDQS0	EDQS0	EDQS2	EDQS2	EDQS0
E09	EDQS0_B	EDQS0_B	EDQS2_B	EDQS2_B	EDQS0_B
B11	EA4	EA3	EA3	EA4	EA4
D15	EBA0	EA12	VDDIO	VDDIO	EBA0
E15	EA2	EBG1	VDDIO	VDDIO	EA2
A16	ERAS	ERAS	EA6	EA7	ERAS
B16	ECAS	ECAS	EA8	EA9	ECAS
B12	EBA1	EBA1	VDDIO	VDDIO	EBA1
A17	EBA2	EBG0	VDDIO	VDDIO	EBA2
B15	ERWE	ERWE	VDDIO	VDDIO	ERWE
F15	EA15	EACT#	EA9	EA8	EA15
B14	EA13	EA2	VDDIO	VDDIO	EA13
B09	EA10	EA9	VDDIO	VDDIO	EA10
A14	EA9	EA8	EA7	EA6	EA9
A09	ECKE	ECKE	ECKE0	ECKE0	ECKE0
B13	EA3	EBA0	VDDIO	VDDIO	EA3
C12	EA0	EA4	EA1	EA1	EA0
A13	EA5	EA6	EA5	EA5	EA5
E12	EA12	EA10	VDDIO	VDDIO	EA12
D12	EA7	EA0	EA0	EA3	EA7
F12	EA11	EA11	EA2	EA2	EA11
A11	EA1	EA5	VDDIO	VDDIO	EA1
C11	EA6	EA1	ECKE1	ECKE1	EA6
B10	EA8	EA7	EA4	EA0	EA8
C10	EA14	EA13	VDDIO	VDDIO	EA14
E11	ECLK0	ECLK0	ECLK0	ECLK0	ECLK0
D11	ECLK0_B	ECLK0_B	ECLK0_B	ECLK0_B	ECLK0_B
D16	ECLK1	ECLK1	N/A	N/A	ECLK1
E16	ECLK1_B	ECLK1_B	N/A	N/A	ECLK1_B
A15	ECS0	ECS0	ECS0	ECS0	ECS0
B17	ECS1	EODT	ECS1	ECS1	ECS1
C16	ERESET	ERESET	N/A	N/A	ERESET
C01	REXTDN	REXTDN	REXTDN	REXTDN	REXTDN

2.1.3 Detailed Pin Description

Table 2-3: Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-4: DI/DO/DIO type

Type	Description
GPIO	General purpose 1.8V IO
KP2KIO	Keypad 2K resistance IO
KP200KIO	Keypad 200K resistance IO
GPIOOD	General purpose 3.3V IO
I2C33IO	I2C IO
I2C5VTIO	SPI IO
MSDCIO	MSDC IO
AGPIO	Analog general purpose 1.8V IO

Table 2-5: DI/DO/DIO: GPIO type specification

Electrical Characteristics and Operating Conditions of 1.8V Applications						
Parameters	**Descriptions**	**Min**	**Typ**	**Max**	**UNIT**	**Note**
VDDIO	Supply voltage of IO power	1.62	1.8	1.98	V	
Inputs						
VIH	Input logic low voltage	0.65*VDDIO		VDDIO+0.3	V	
VIL	Input logic high voltage	-0.3		0.35*VDDIO	V	
Rpu	Input pull-up resistance	40	75	190	Kohm	
Rpd	Input pull-down resistance	40	75	190	Kohm	
Outputs						

Electrical Characteristics and Operating Conditions of 1.8V Applications						
VOH(DC)	DC Output logic low voltage	0.75*VDDIO			V	
VOL(DC)	DC Output logic high voltage			0.25*VDDIO	V	

Table 2-6: DIO: KP2KIO type specification

Electrical Characteristics and Operating Conditions of 1.8V Applications						
Parameters	**Descriptions**	**Min**	**Typ**	**Max**	**UNIT**	**Note**
VDDIO	Supply voltage of IO power	1.62	1.8	1.98	V	
Inputs						
VIH	Input logic low voltage	0.65*VDDIO		VDDIO+0.3	V	
VIL	Input logic high voltage	-0.3		0.35*VDDIO	V	
Rpu	Input pull-up resistance			2	Kohm	
Rpd	Input pull-down resistance			2	Kohm	
Outputs						
VOH(DC)	DC Output logic low voltage	0.75*VDDIO			V	
VOL(DC)	DC Output logic high voltage			0.25*VDDIO	V	

Table 2-7: 2Kohm type Pull up/down Setting

E	Pu/Pd	R1	R0	R value
0	0	0	0	High-Z
0	0	0	1	PU-75k
0	0	1	0	PU-2k
0	0	1	1	PU-75k/2k
0	1	0	0	High-Z

E	Pu/Pd	R1	Ro	R value
0	1	0	1	PD-75k
0	1	1	0	PD-2k
0	1	1	1	PD-75k/2k
1	X	X	X	High-Z

Table 2-8: DIO: KP200KIO type specification

Electrical Characteristics and Operating Conditions of 1.8V Applications						
Parameters	**Descriptions**	**Min**	**Typ**	**Max**	**UNIT**	**Note**
VDDIO	Supply voltage of IO power	1.62	1.8	1.98	V	
Inputs						
VIH	Input logic low voltage	0.65*VDDIO		VDDIO+0.3	V	
VIL	Input logic high voltage	-0.3		0.35*VDDIO	V	
Rpu	Input pull-up resistance	200			Kohm	
Rpd	Input pull-down resistance	200			Kohm	
Outputs						
VOH(DC)	DC Output logic low voltage	0.75*VDDIO			V	
VOL(DC)	DC Output logic high voltage			0.25*VDDIO	V	

Table 2-9: 200Kohm type Pull up/down Setting

E	Pu/Pd	R1	Ro	R value
0	0	0	0	High-Z
0	0	0	1	PU-75k
0	0	1	0	PU-200k

E	Pu/Pd	R1	Ro	R value
0	0	1	1	PU-75k/200k
0	1	0	0	High-Z
0	1	0	1	PD-75k
0	1	1	0	PD-200k
0	1	1	1	PD-75k/200k
1	X	X	X	High-Z

Table 2-10: DIO: GPIOOD type specification

Operating Conditions of 3.3V Applications						
Parameters	**Descriptions**	**Min**	**Typ**	**Max**	**UNIT**	**Note**
VCC3IO	Supply voltage of SD IO power	2.97	3.3	3.63	V	
Outputs						
VOH(DC)	DC Output logic low voltage	VCC3IO-0.4V		VCC3IO+0.3	V	VCC3IO=min, IOH= - 2mA
VOL(DC)	DC Output logic high voltage	-0.3		0.4	V	VCC3IO=min, IOL= -2mA
Inputs						
VIH	Input logic low voltage	2.0		VCC3IO+0.3	V	
VIL	Input logic high voltage	-0.3		0.8	V	
Rpu1	Input pull-up resistance	40	75	190	Kohm	control pin PU=1
Rpd1	Input pull-down resistance	40	75	190	Kohm	control pin PD=1

Operating Conditions of 1.8V Applications						
Parameters	Descriptions	Min	Typ	Max	UNIT	Note
VCC3IOIO	Supply voltage of SIM IO power	1.7	1.8	1.9	V	
Outputs						

Operating Conditions of 1.8V Applications						
IO Voh	IO output Ioh=1mA	VCC3IO-0.2		VCC3IO+0.3	V	
IO Vol	IO output Iol=-1mA	-0.3		0.2	V	
Inputs						
VIH	Input logic low voltage	1.27		VCC3IO+0.3	V	
VIL	Input logic high voltage	-0.3		0.58	V	
Rpu1	Input pull-up resistance	10	50	100	Kohm	control pin PU=1
Rpd1	Input pull-down resistance	10	50	100	Kohm	control pin PD=1

Table 2-11: DIO: I2C33IO type specification

Electrical Characteristics and Operating Conditions of 1.8V Applications						
Parameters	**Descriptions**	**Min**	**Typ**	**Max**	**UNIT**	**Note**
VDDIO	Supply voltage of IO power	1.62	1.8	1.98	V	
Inputs						
VIH	Input logic low voltage	0.65*VDDIO		VDDIO+0.3	V	
VIL	Input logic high voltage	-0.3		0.35*VDDIO	V	
Rpd	Input pull-down resistance	40	75	350	Kohm	
Outputs						
VOL(DC)	DC Output logic low voltage (VIN>=2V)			0.4	V	
VOL(DC)	DC Output logic low voltage (VIN<2V)			0.2*VDDIO	V	
External Pull-up Resistance						
Rpull-up	External Pull-up resistance		1.0		Kohm	

Table 2-12: DIO: I2C5VTIO type specification

Electrical Characteristics and Operating Conditions of 1.8V Applications						
Parameters	**Descriptions**	**Min**	**Typ**	**Max**	**UNIT**	**Note**
VDDIO	Supply voltage of IO power	1.62	1.8	1.98	V	
Inputs						
VIH	Input logic low voltage	0.65*VDDIO		VDDIO+0.3	V	
VIL	Input logic high voltage	-0.3		0.35*VDDIO	V	
Rpd	Input pull-down resistance	40	75	550	Kohm	
Outputs						
VOL(DC)	DC Output logic low voltage			0.2*VDDIO	V	
IOL(DC)	DC Output logic low current	3			mA	
External Pull-up Resistance						
Rpull-up	External Pull-up resistance		1.0		Kohm	

Table 2-13: DIO: MSDCIO type specifications

Operating Conditions of 3.3V Applications						
Parameters	**Descriptions**	**Min**	**Typ**	**Max**	**UNIT**	**Note**
VCC3IO	Supply voltage of SD IO power	2.97	3.3	3.63	V	
Outputs						
IO Voh	IO output Ioh=2mA	0.75*VCC3IO		VCC3IO+0.3	V	
IO Vol	IO output Iol=-2mA	-0.3		0.125*VCC3IO	V	

Operating Conditions of 3.3V Applications						
Inputs						
VIH	Input logic low voltage	0.625*VCC3IO		VCC3IO+0.3	V	
VIL	Input logic high voltage	-0.3		0.25*VCC3IO	V	
Rpu1	Input pull-up resistance	10	50	100	Kohm	control pin R0=0, R1=1
Rpd1	Input pull-down resistance	10	50	100	Kohm	control pin R0=0, R1=1
Rpu0	Input pull-up resistance	5	7.5	10	Kohm	control pin R0=1, R1=0
Rpd0	Input pull-down resistance	5	7.5	10	Kohm	control pin R0=1, R1=0

Operating Conditions of 1.8V Applications						
Parameters	**Descriptions**	**Min**	**Typ**	**Max**	**UNIT**	**Note**
VCC3IOIO	Supply voltage of SIM IO power	1.7	1.8	1.9	V	
Outputs						
IO Voh	IO output Ioh=1mA	VCC3IO-0.45		VCC3IO+0.3	V	
IO Vol	IO output Iol=-1mA	-0.3		0.45	V	
Inputs						
VIH	Input logic low voltage	0.65*VCC3IO		VCC3IO+0.3	V	
VIL	Input logic high voltage	-0.3		0.35*VCC3IO	V	
Rpu1	Input pull-up resistance	10	50	100	Kohm	4, control pin R0=0, R1=1

Operating Conditions of 1.8V Applications						
Rpd1	Input pull-down resistance	10	50	100	Kohm	4, control pin R0=0, R1=1
Rpu0	Input pull-up resistance	5	7.5	10	Kohm	4, control pin R0=1, R1=0
Rpd0	Input pull-down resistance	5	7.5	10	Kohm	4, control pin R0=1, R1=0

Table 2-14: DIO: AGPIO type specification

Electrical Characteristics and Operating Conditions of 1.8V Applications						
Parameters	Descriptions	Min	Typ	Max	UNIT	Note
VDDIO	Supply voltage of IO power	1.62	1.8	1.98	V	
Inputs						
VIH	Input logic low voltage	0.65*VDDIO		VDDIO+0.3	V	
VIL	Input logic high voltage	-0.3		0.35*VDDIO	V	
Rpu	Input pull-up resistance	40	75	190	Kohm	
Rpd	Input pull-down resistance	40	75	190	Kohm	
Outputs						
VOH(DC)	DC Output logic low voltage	0.75*VDDIO			V	
VOL(DC)	DC Output logic high voltage			0.25*VDDIO	V	

Table 2-15: Detailed pin description

Pin name	Type	DI/DO/DIO type	Description	Power domain
SYSTEM				
SYSRSTB	DI	GPIO	System reset input	DVDD18_IO3
WATCHDOG	DIO	GPIO	Watchdog reset output	DVDD18_IO3
TESTMODE	DI	GPIO	Test mode	DVDD18_IO1
RTC32K_CK	DIO	GPIO	32K clock input	DVDD18_IO3
SRCLKENA	DIO	GPIO	26MHz co-clock enable output	DVDD18_IO3
PMIC				
PWRAP_SPI0_MO	DIO	GPIO	PMIC SPI control interface	DVDD18_IO3
PWRAP_SPI0_MI	DIO	GPIO	PMIC SPI control interface	DVDD18_IO3
PWRAP_SPI0_CSN	DIO	GPIO	PMIC SPI control interface	DVDD18_IO3
PWRAP_SPI0_CK	DIO	GPIO	PMIC SPI control interface	DVDD18_IO3
PWRAP_INT	DIO	GPIO	PMIC SPI control interface	DVDD18_IO3
JTAG				
JTCK	DIO	GPIO	JTCK	DVDD18_IO1
JTDO	DIO	GPIO	JTDO	DVDD18_IO1
JTDI	DIO	GPIO	JTDI	DVDD18_IO1
JTMS	DIO	GPIO	JTMS	DVDD18_IO1
LCD				
DISP_PWM	DIO	GPIO	Display PWM output	DVDD18_IO1
DSI_TE	DIO	GPIO	DSI tearing effect control	DVDD18_IO1
LCM_RST	DIO	GPIO	LCM reset	DVDD18_IO1
KeyPad				
KPCOL0	DIO	KP200KIO	Key Pad column 0	DVDD18_IO1
KPCOL1	DIO	KP200KIO	Key Pad column 1	DVDD18_IO1
KPROW0	DIO	KP2KIO	Key Pad raw 0	DVDD18_IO1
KPROW1	DIO	KP2KIO	Key Pad raw 1	DVDD18_IO1
I2S				
I2S_DATA_IN	DIO	GPIO	I2S data input pin	DVDD18_IO1
I2S_BCK	DIO	GPIO	I2S clock	DVDD18_IO1
I2S_LRCK	DIO	GPIO	I2S word select	DVDD18_IO1
I2S merge interface				
MRG_DO	DIO	GPIOOD	MTK audio interface	DVDD28_DPI
MRG_CLK	DIO	GPIOOD	MTK audio interface	DVDD28_DPI
MRG_DI	DIO	GPIOOD	MTK audio interface	DVDD28_DPI
MRG_SYNC	DIO	GPIOOD	MTK audio interface	DVDD28_DPI
EINT				
EINT0	DIO	GPIOOD	External interrupt 0	DVDD28_DPI
EINT1	DIO	GPIOOD	External interrupt 1	DVDD28_DPI
EINT2	DIO	GPIOOD	External interrupt 2	DVDD28_DPI
EINT3	DIO	GPIOOD	External interrupt 3	DVDD28_DPI
EINT4	DIO	GPIOOD	External interrupt 4	DVDD28_DPI
EINT5	DIO	GPIOOD	External interrupt 5	DVDD28_DPI
EINT6	DIO	GPIOOD	External interrupt 6	DVDD28_DPI

Pin name	Type	DI/DO/DIO type	Description	Power domain
EINT7	DIO	GPIOOD	External interrupt 7	DVDD28_DPI
EINT8	DIO	GPIOOD	External interrupt 8	DVDD28_DPI
EINT9	DIO	GPIOOD	External interrupt 9	DVDD28_DPI
EINT10	DIO	GPIOOD	External interrupt 10	DVDD28_DPI
EINT11	DIO	GPIOOD	External interrupt 11	DVDD28_DPI
EINT12	DIO	GPIOOD	External interrupt 12	DVDD28_DPI
EINT13	DIO	GPIOOD	External interrupt 13	DVDD28_DPI
EINT18	DIO	GPIOOD	External interrupt 18	DVDD18_IO2
EINT19	DIO	GPIOOD	External interrupt 19	DVDD18_IO2
EINT20	DIO	GPIOOD	External interrupt 20	DVDD18_IO2
EINT24	DIO	GPIOOD	External interrupt 24	DVDD28_DPI
EINT25	DIO	GPIOOD	External interrupt 25	DVDD28_DPI
UART				
URXD0	DIO	AGPIO	UART0 RX	DVDD18_IO1
UTXD0	DIO	AGPIO	UART0 TX	DVDD18_IO1
URXD1	DIO	AGPIO	UART1 RX	DVDD18_IO1
UTXD1	DIO	AGPIO	UART1 TX	DVDD18_IO1
URXD2	DIO	AGPIO	UART2 RX	DVDD28_DPI
UTXD2	DIO	AGPIO	UART2 TX	DVDD28_DPI
SPI				
SPI_CS	DIO	GPIO	SPI chip select	DVDD18_IO2
SPI_MI	DIO	GPIO	SPI data in	DVDD18_IO2
SPI_MO	DIO	GPIO	SPI data out	DVDD18_IO2
SPI_CK	DIO	GPIO	SPI clock	DVDD18_IO2
NAND Flash Interface				
EINT14	DIO	MSDCIO	NCLE	DVDD28_NFI
EINT15	DIO	MSDCIO	NCEB1	DVDD28_NFI
EINT16	DIO	MSDCIO	NCEB0	DVDD28_NFI
EINT17	DIO	MSDCIO	NREB	DVDD28_NFI
EINT21	DIO	MSDCIO	NRNB	DVDD28_NFI
EINT22	DIO	MSDCIO	NRE_C	DVDD28_NFI
EINT23	DIO	MSDCIO	NDQS_C	DVDD28_NFI
MSDC0				
MSDC0_DAT7	DIO	MSDCIO	MSDC0 data7 pin / NLD7	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_DAT6	DIO	MSDCIO	MSDC0 data6 pin / NLD6	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_DAT5	DIO	MSDCIO	MSDC0 data5 pin / NLD4	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_RSTB	DIO	MSDCIO	MSDC0 reset output /NLD0	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_DAT4	DIO	MSDCIO	MSDC0 data4 pin / NLD3	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_DAT2	DIO	MSDCIO	MSDC0 data2 pin / NLD5	DVDD28_MSDC0 / DVDD18_IO3

Pin name	Type	DI/DO/DIO type	Description	Power domain
MSDC0_DAT3	DIO	MSDCIO	MSDC0 data3 pin / NLD1	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_CMD	DIO	MSDCIO	MSDC0 command pin / NALE	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_CLK	DIO	MSDCIO	MSDC0 clock output / NWEB	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_DAT1	DIO	MSDCIO	MSDC0 data1 pin / NLD8	DVDD28_MSDC0 / DVDD18_IO3
MSDC0_DAT0	DIO	MSDCIO	MSDC0 data0 pin / NLD2	DVDD28_MSDC0 / DVDD18_IO3
MSDC1				
MSDC1_CLK	DIO	MSDCIO	MSDC1 clock output	DVDD28_MSDC1
MSDC1_CMD	DIO	MSDCIO	MSDC1 command pin	DVDD28_MSDC1
MSDC1_DAT0	DIO	MSDCIO	MSDC1 data0 pin	DVDD28_MSDC1
MSDC1_DAT1	DIO	MSDCIO	MSDC1 data1 pin	DVDD28_MSDC1
MSDC1_DAT2	DIO	MSDCIO	MSDC1 data2 pin	DVDD28_MSDC1
MSDC1_DAT3	DIO	MSDCIO	MSDC1 data3 pin	DVDD28_MSDC1
MSDC2				
MSDC2_CLK	DIO	MSDCIO	MSDC2 clock output	DVDD28_MSDC2
MSDC2_CMD	DIO	MSDCIO	MSDC2 command pin	DVDD28_MSDC2
MSDC2_DAT0	DIO	MSDCIO	MSDC2 data0 pin	DVDD28_MSDC2
MSDC2_DAT1	DIO	MSDCIO	MSDC2 data1 pin	DVDD28_MSDC2
MSDC2_DAT2	DIO	MSDCIO	MSDC2 data2 pin	DVDD28_MSDC2
MSDC2_DAT3	DIO	MSDCIO	MSDC2 data3 pin	DVDD28_MSDC2
EFUSE				
FSOURCE_P	P		E-FUSE blowing power control	DVDD18_EFUSE
EMI				
ECLK0	AIO		DRAM clock 0 output	VCCIO
ECLK0_B	AIO		DRAM clock 0 output #	VCCIO
ECLK1	AIO		DRAM clock 1 output	VCCIO
ECLK1_B	AIO		DRAM clock 1 output #	VCCIO
ECKE	AIO		DRAM command output CKE	VCCIO
ECS0	AIO		DRAM chip select 0 #	VCCIO
ECS1	AIO		DRAM chip select 1 #	VCCIO
ECAS	AIO		DRAM cmd column strobe output	VCCIO
ERAS	AIO		DRAM cmd row strobe ouput	VCCIO
ERESET	AIO		DRAM reset pin	VCCIO
ERWE	AIO		DRAM cmd write enable	VCCIO
EA0	AIO		DRAM address output 0	VCCIO
EA1	AIO		DRAM address output 1	VCCIO
EA2	AIO		DRAM address output 2	VCCIO
EA3	AIO		DRAM address output 3	VCCIO
EA4	AIO		DRAM address output 4	VCCIO
EA5	AIO		DRAM address output 5	VCCIO
EA6	AIO		DRAM address output 6	VCCIO

Pin name	Type	DI/DO/DIO type	Description	Power domain
EA7	AIO		DRAM address output 7	VCCIO
EA8	AIO		DRAM address output 8	VCCIO
EA9	AIO		DRAM address output 9	VCCIO
EA10	AIO		DRAM address output 10	VCCIO
EA11	AIO		DRAM address output 11	VCCIO
EA12	AIO		DRAM address output 12	VCCIO
EA13	AIO		DRAM address output 13	VCCIO
EA14	AIO		DRAM address output 14	VCCIO
EA15	AIO		DRAM address output 15	VCCIO
EBA0	AIO		DRAM banks address	VCCIO
EBA1	AIO		DRAM banks address	VCCIO
EBA2	AIO		DRAM banks address	VCCIO
EDQM0	AIO		DRAM DQM 0	VCCIO
EDQM1	AIO		DRAM DQM 1	VCCIO
EDQM2	AIO		DRAM DQM 2	VCCIO
EDQM3	AIO		DRAM DQM 3	VCCIO
EDQS0	AIO		DRAM DQS 0	VCCIO
EDQS0_B	AIO		DRAM DQS 0 #	VCCIO
EDQS1	AIO		DRAM DQS 1	VCCIO
EDQS1_B	AIO		DRAM DQS 1 #	VCCIO
EDQS2	AIO		DRAM DQS 2	VCCIO
EDQS2_B	AIO		DRAM DQS 2 #	VCCIO
EDQS3	AIO		DRAM DQS 3	VCCIO
EDQS3_B	AIO		DRAM DQS 3 #	VCCIO
ED0	AIO		DRAM data pin 0	VCCIO
ED1	AIO		DRAM data pin 1	VCCIO
ED2	AIO		DRAM data pin 2	VCCIO
ED3	AIO		DRAM data pin 3	VCCIO
ED4	AIO		DRAM data pin 4	VCCIO
ED5	AIO		DRAM data pin 5	VCCIO
ED6	AIO		DRAM data pin 6	VCCIO
ED7	AIO		DRAM data pin 7	VCCIO
ED8	AIO		DRAM data pin 8	VCCIO
ED9	AIO		DRAM data pin 9	VCCIO
ED10	AIO		DRAM data pin 10	VCCIO
ED11	AIO		DRAM data pin 11	VCCIO
ED12	AIO		DRAM data pin 12	VCCIO
ED13	AIO		DRAM data pin 13	VCCIO
ED14	AIO		DRAM data pin 14	VCCIO
ED15	AIO		DRAM data pin 15	VCCIO
ED16	AIO		DRAM data pin 16	VCCIO
ED17	AIO		DRAM data pin 17	VCCIO
ED18	AIO		DRAM data pin 18	VCCIO

Pin name	Type	DI/DO/DIO type	Description	Power domain
ED19	AIO		DRAM data pin 19	VCCIO
ED20	AIO		DRAM data pin 20	VCCIO
ED21	AIO		DRAM data pin 21	VCCIO
ED22	AIO		DRAM data pin 22	VCCIO
ED23	AIO		DRAM data pin 23	VCCIO
ED24	AIO		DRAM data pin 24	VCCIO
ED25	AIO		DRAM data pin 25	VCCIO
ED26	AIO		DRAM data pin 26	VCCIO
ED27	AIO		DRAM data pin 27	VCCIO
ED28	AIO		DRAM data pin 28	VCCIO
ED29	AIO		DRAM data pin 29	VCCIO
ED30	AIO		DRAM data pin 30	VCCIO
ED31	AIO		DRAM data pin 31	VCCIO
REXTDN	AIO		DRAM REXTDN pin	VCCIO
RTN	AIO		NC	VCCIO
RTP	AIO		DRAM voltage reference 2, connected to ½ VCCIO	VCCIO
CAM				
CMPCLK	DIO	GPIO	Pixel clock from sensor	DVDD18_IO0
CMMCLK	DIO	GPIO	Master clock to sensor	DVDD18_IO0
CMDAT0	DIO	GPIO	CAM sensor Data0	DVDD18_IO0
CMDAT1	DIO	GPIO	CAM sensor Data1	DVDD18_IO0
I2C0				
SCL0	DIO	I2C33IO	I2C0 clock	DVDD18_IO1
SDA0	DIO	I2C33IO	I2C0 data	DVDD18_IO1
I2C1				
SCL1	DIO	I2C33IO	I2C1 clock	DVDD18_IO1
SDA1	DIO	I2C33IO	I2C1 data	DVDD18_IO1
I2C2				
SCL2	DIO	I2C33IO	I2C2 clock	DVDD18_IO3
SDA2	DIO	I2C33IO	I2C2 data	DVDD18_IO3
XO				
XO_IN	AIO		26MHz clock input for AP	AVDD22_XO
CLKO_26M	AIO		26MHz clock output to PMIC	AVDD22_XO
CLKO_32K	AIO		32KHz clock output to PMIC	AVDD22_XO_32K
ABB				
REFP	AIO		Positive reference port for internal circuit	AVDD18_AP
AUX_IN0	AIO		AuxADC external input channel 0	AVDD18_AP
AUX_IN1	AIO		AuxADC external input channel 1	AVDD18_AP
AUX_IN2	AIO		AuxADC external input channel 2	AVDD18_AP
AUX_IN3	AIO		AuxADC external input channel 3	AVDD18_AP
AUX_IN4	AIO		AuxADC external input channel 4	AVDD18_AP
AUX_IN5	AIO		AuxADC external input channel 5	AVDD18_AP

Pin name	Type	DI/DO/DIO type	Description	Power domain
WBT				
WB_RFIN	AIO		WF/BT RF IO port	AVDD33_WBT
MIPI				
TDN3	AIO		DSI0 lane3 N / LVDSTX lane3 N	DVDD18_MIPITX
TDP3	AIO		DSI0 lane3 P / LVDSTX lane3 P	DVDD18_MIPITX
TDN2	AIO		DSI0 lane2 N / LVDSTX CK lane N	DVDD18_MIPITX
TDP2	AIO		DSI0 lane2 P / LVDSTX CK lane P	DVDD18_MIPITX
TCN	AIO		DSI0 CK lane N / LVDSTX lane2 N	DVDD18_MIPITX
TCP	AIO		DSI0 CK lane P / LVDSTX lane2 P	DVDD18_MIPITX
TDN1	AIO		DSI0 lane1 N / LVDSTX lane1 N	DVDD18_MIPITX
TDP1	AIO		DSI0 lane1 P / LVDSTX lane1 P	DVDD18_MIPITX
TDN0	AIO		DSI0 lane0 N / LVDSTX lane0 N	DVDD18_MIPITX
TDP0	AIO		DSI0 lane0 P / LVDSTX lane0 P	DVDD18_MIPITX
VRT	AO		External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground	DVDD18_MIPITX
RDN3	AIO		CSI0 lane3 N / CAM sensor Data4	DVDD18_MIPIRX
RDP3	AIO		CSI0 lane3 P / CAM sensor Data5	DVDD18_MIPIRX
RDN2	AIO		CSI0 lane2 N / CAM sensor Data8	DVDD18_MIPIRX
RDP2	AIO		CSI0 lane2 P / CAM sensor Data9	DVDD18_MIPIRX
RCN	AIO		CSI0 CK lane N	DVDD18_MIPIRX
RCP	AIO		CSI0 CK lane P	DVDD18_MIPIRX
RDN1	AIO		CSI0 lane1 N	DVDD18_MIPIRX
RDP1	AIO		CSI0 lane1 P	DVDD18_MIPIRX
RDN0	AIO		CSI0 lane0 N	DVDD18_MIPIRX
RDP0	AIO		CSI0 lane0 P	DVDD18_MIPIRX
RDN1_A	AIO		CSI1 lane1 N / CAM sensor Data2	DVDD18_MIPIRX
RDP1_A	AIO		CSI1 lane1 P / CAM sensor Data3	DVDD18_MIPIRX
RCN_A	AIO		CSI1 CK lane N / CAM sensor Data6	DVDD18_MIPIRX
RCP_A	AIO		CSI1 CK lane P / CAM sensor Data7	DVDD18_MIPIRX
RDN0_A	AIO		CSI1 lane0 N / CAM sensor HSYNC	DVDD18_MIPIRX
RDP0_A	AIO		CSI1 lane0 P / CAM sensor VSYNC	DVDD18_MIPIRX
USB				
USB_DP_P0	AIO		USB port0 D+ differential data line	AVDD33_USB
USB_DM_P0	AIO		USB port0 D- differential data line	AVDD33_USB
CHD_DP_P0	AIO		BC1.1 Charger DP	AVDD33_USB
CHD_DM_P0	AIO		BC1.1 Charger DM	AVDD33_USB
USB_VRT_P0	AO		USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
USB_VBUS_P0	AI		Power for connected device	AVDD18_USB
USB_DP_P1	AIO		USB port1 D+ differential data line	AVDD33_USB
USB_DM_P1	AIO		USB port1 D- differential data line	AVDD33_USB
HDMI Transmitter				
CEC	DIO	I2C5VTIO	HDMITX CEC	DVDD18_IO2

Pin name	Type	DI/DO/DIO type	Description	Power domain
HTPLG	DIO	I2C5VTIO	HDMITX Hot Plug Detection Pin	DVDD18_IO2
HDMISCK	DIO	I2C5VTIO	HDMITX I2C clock pin	DVDD18_IO2
HDMISD	DIO	I2C5VTIO	HDMITX I2C data pin	DVDD18_IO2
HDMITX_REXT	AIO		External resistor for HDMITX bias	AVDD18_HDMITX
HDMITX_CLK_M	AIO		HDMITX channel CK M	AVDD18_HDMITX
HDMITX_CLK_P	AIO		HDMITX channel CK P	AVDD18_HDMITX
HDMITX_CH0_M	AIO		HDMITX channel 0 M	AVDD18_HDMITX
HDMITX_CH0_P	AIO		HDMITX channel 0 P	AVDD18_HDMITX
HDMITX_CH1_M	AIO		HDMITX channel 1 M	AVDD18_HDMITX
HDMITX_CH1_P	AIO		HDMITX channel 1 P	AVDD18_HDMITX
HDMITX_CH2_M	AIO		HDMITX channel 2 M	AVDD18_HDMITX
HDMITX_CH2_P	AIO		HDMITX channel 2 P	AVDD18_HDMITX
Audio Codec				
ACCDET	AIO		Accessory detection input	AVDD28_AUDIO
AU_MICBIAS1	AIO		Microphone bias for earphone	AVDD28_AUDIO
AU_MICBIAS0	AIO		Microphone bias for main and 2nd microphone	AVDD28_AUDIO
AU_VIN0_P	AIO		Audio analog input 1 positive port	AVDD22_AUDIO
AU_VIN0_N	AIO		Audio analog input 1 negative port	AVDD22_AUDIO
AU_VIN1_P	AIO		Audio analog input 2 positive port	AVDD22_AUDIO
AU_VIN1_N	AIO		Audio analog input 2 negative port	AVDD22_AUDIO
AU_VIN2_P	AIO		Audio analog input 3 positive port	AVDD22_AUDIO
AU_VIN2_N	AIO		Audio analog input 3 negative port	AVDD22_AUDIO
AU_LOLN	AIO		Lineout N to drive SPK AMP	AVDD28_AUDIO
AU_LOLP	AIO		Lineout P to drive SPK AMP	AVDD28_AUDIO
AU_HPL	AIO		L-CH headphone output	AVDD28_AUDIO
AU_HPR	AIO		R-CH headphone output	AVDD28_AUDIO
AU_TN	AIO		Audio Codec Test Pin N	AVDD22_AUDIO
AU_TP	AIO		Audio Codec Test Pin P	AVDD22_AUDIO
Analog power				
AVDD18_PLLGP	P		Analog power input 1.8V for PLL and oscillator	-
AVDD18_AP	P		Analog power input 1.8V for AuxADC, TSENSE	-
AVDD18_MEMPLL	P		Analog power for MEMPLL	-
AVDD18_WBT	P		Analog power 1.8V for WBT RF	-
AVDD18_WBT_AFE	P		Analog power 1.8V for WBT AFE	-
AVDD33_WBT	P		Analog power 3.5V (default) for WBT TX PA and IQM	-
AVDD18_MIPITX	P		Analog power for MIPI DSI	-
AVDD18_MIPIRX	P		Analog power for MIPI CSI	-
AVDD18_HDMITX	P		Analog power input 1.8V for HDMI/MHL transmitter	-
AVDD18_USB	P		Analog power 1.8V for USB	-
AVDD33_USB	P		Analog power 3.3V for USB	-

Pin name	Type	DI/DO/DIO type	Description	Power domain
AVDD22_AUDIO	P		Analog power 2.2V for AUDIO CODEC	-
AVDD28_AUDIO	P		Analog power 2.8V for AUDIO CODEC	-
AVDD22_XO	P		Analog power 2.2V for Crystal Oscillator	-
AVDD22_XO_32K	P		Analog power 2.2V for 32K output clock buffer	-
Digital power				
DVDD18_IO0	P		Digital power input for IO	-
DVDD18_IO1	P		Digital power input for IO	-
DVDD18_IO2	P		Digital power input for IO	-
DVDD18_IO3	P		Digital power input for IO	-
DVDD18_EFUSE	P		Digital power input for efuse IO	-
DVDD28_MSDC0	P		Digital power input for 1.8V/3.3V MSDC0/NAND flash IO	-
DVDD28_DPI	P		Digital power input for 3.3V DPI IO	-
DVDD28_NFI	P		Digital power input for 3.3V NAND Flash IO	-
DVDD28_MSDC1	P		Digital power input for 1.8/3.3V MSDC IO	-
DVDD28_MSDC2	P		Digital power input for 1.8/3.3V MSDC IO	-
VCCIO	P		Digital power input for 1.24V/1.39V/2.5V EMI	-
VCCK	P		Digital power input for core	-
VCCK_VPROC	P		Digital power input for processor	-
Analog ground				
AVSS18_PLLGP	G		Analog ground for PLL	-
AVSS18_AP	G		Analog ground for AuxADC, TSENSE	-
AVSS22_XO	G		Analog ground for Crystal Oscillator	-
AVSS22_XO_32K	G		Analog ground for 32K output clock buffer	-
AVSS_CONN	G		Analog ground for connectivity RF	-
AVSS18_HDMITX	G		Analog ground for HDMI/MHL tranmitter	-
AVSS18_MIPI	G		Analog ground for MIPI	-
AVSS_AUDIO	G		Analog ground for Audio Codec	-
AVSS33_USB	G		Analog ground for USB	-
Digital ground				
GNDK	G		Digital ground	-

This product can't support Camera, HDMI, MIPI DSI and CSI, DSP_PWM, LCM_RST, DPI, the related pin you can only as the GPI or GPIO function.

2.1.4 Interface Application Notice

Table 2-16: Interface Application Notice

Interface Types	Total Sets	Interface with Non-MTK IC	Constraints
I2C	3	Y	Max speed 1 MHz
PWRAP SPI (PMIC SPI)	1	N	
SPI interface	1	Y	N/A
UART	3	Y	N/A
Key pad	1	Y	
USB2.0	2	Y	N/A
Nand Flash/MSDC0/eMMC	1	Y	
MSDC1/SPI NOR	1	Y	
MSDC2 (SDIO)	1	Y	Need external GPIO for sleep wake-up
Ethernet MII/RMII	1	Y	N/A
Audio I2S 8-CH Output	1	Y	Only master mode
Audio I2S 2-CH Input	1	Y	Slave mode max input rate support <= 48K
Audio PCM	1	Y	8K/16K/32K
Audio TDM (RX)	1	Y	Master mode only Support one data pin for multi-channel input (max channel=8)

2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 2-17: Absolute maximum ratings for power supply

Symbol or Pin name	Description	Min.	Max.	Unit
AVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AUXADC, TSENSE	1.7	1.9	V
AVDD18_WBT	Analog power 1.8V for WBT RF	1.7	1.9	V
AVDD18_WBT_AFE	Analog power 1.8V for WBT AFE	1.7	1.9	V
AVDD33_WBT	Analog power 3.5V (default) for WBT TX PA and IQM	3.3	3.6	V
AVDD18_ANA	Analog power	1.7	1.9	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.9	V
AVDD18_MEMPLL	Analog power for MEMPLL	1.7	1.9	V
AVDD22_AUDIO	Analog power 2.2V for AUDIO CODEC	2.1	2.3	V
AVDD28_AUDIO	Analog power 2.8V for AUDIO CODEC	2.7	2.9	V
AVDD22_XO	Analog power 2.2V for Crystal Oscillator	2.1	2.3	V
AVDD22_XO_32K	Analog power 2.2V for 32K output clock buffer	2.1	2.3	V
DVDD18_IO0	Digital power input for IO	1.7	1.9	V

Symbol or Pin name	Description	Min.	Max.	Unit
DVDD18_IO1	Digital power input for IO	1.7	1.9	V
DVDD18_IO2	Digital power input for IO	1.7	1.9	V
DVDD18_IO3	Digital power input for IO	1.7	1.9	V
DVDD18_EFUSE	Digital power input for efuse IO	1.8	2.2	V
DVDD28_MII	Digital power input for MII IO	1.7	3.63	V
DVDD28_NFI	Digital power input for NAND flash IO	1.7	3.63	V
DVDD28_MSDC0	Digital power input for EMMC/NAND flash IO	1.7	3.63	V
DVDD28_MSDC1	Digital power input for MSDC1 IO	1.7	3.63	V
DVDD28_MSDC2	Digital power input for MSDC2 IO	1.7	3.63	V
VCCIO	Digital power input for EMI	1.14	1.575	V
VCCK	Digital power input for core	0.765	1.31	V
VCCK_VPROC	Digital power input for CPU	0.765	1.31	V

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.

2.2.2 Recommended Operating Conditions

Table 2-18: Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_PLLGP	Analog power input 1.8V for PLL	1.7	1.8	1.9	V
AVDD18_AP	Analog power input 1.8V for AUXADC, TSENSE	1.7	1.8	1.9	V
AVDD18_WBT	Analog power 1.8V for WBT RF	1.7	1.8	1.9	V
AVDD18_WBT_AFE	Analog power 1.8V for WBT AFE	1.7	1.8	1.9	V
AVDD33_WBT	Analog power 3.5V (default) for WBT TX PA and IQM	3.3	3.5	3.6	V
AVDD18_ANA	Analog power	1.7	1.8	1.9	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.3	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.8	1.9	V
AVDD18_MEMPLL	Analog power for MEMPLL	1.7	1.8	1.9	V
AVDD22_AUDIO	Analog power 2.2V for AUDIO CODEC	2.1	2.2	2.3	V
AVDD28_AUDIO	Analog power 2.8V for AUDIO CODEC	2.7	2.8	2.9	V
AVDD22_XO	Analog power 2.2V for Crystal Oscillator	2.1	2.2	2.3	V
AVDD22_XO_32K	Analog power 2.2V for 32K output clock buffer	2.1	2.2	2.3	V
DVDD18_IO0	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_IO1	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_IO2	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_IO3	Digital power input for IO	1.7	1.8	1.9	V
DVDD18_EFUSE	Digital power input for efuse IO	1.8	2.0	2.2	V
DVDD28_MII	Digital power input for MII IO	1.7	1.8	1.9	V
		2.52	2.8	3.08	
		2.97	3.3	3.63	

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD28_NFI	Digital power input for NAND flash IO	1.7	1.8	1.9	V
		2.52	2.8	3.08	
		2.97	3.3	3.63	
DVDD28_MSDC0	Digital power input for EMMC/NAND flash IO	1.7	1.8	1.9	V
		2.52	2.8	3.08	
		2.97	3.3	3.63	
DVDD28_MSDC1	Digital power input for MSDC1 IO	1.7	1.8	1.9	V
		2.52	2.8	3.08	
		2.97	3.3	3.63	
DVDD28_MSDC2	Digital power input for MSDC2 IO	1.7	1.8	1.9	V
		2.52	2.8	3.08	
		2.97	3.3	3.63	
VCCIO	Digital power input for EMI (DDR4)	1.14	1.2	1.26	V
	Digital power input for EMI (DDR3L)	1.283	1.35	1.42	
	Digital power input for EMI (DDR3)	1.425	1.5	1.575	
	Digital power input for EMI (LPDDR2/3)	1.14	1.2	1.26	
VCCK	Digital power input for core	0.765	1.15	1.31	V
VCCK_VPROC	Digital power input for processor	0.765	1.15	1.31	V

2.2.3 Storage Conditions

- Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
- After bag opened, devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing must be:
- Mounted within 168 hours at factory conditions of 30°C/60% RH, or
- Stored at 20% RH.
- Devices require baking before mounting, if:
- Humidity Indicator Card is >20% when read at 23°C+/- 5°C or
- 2a or 2b is not met.
- If baking is required, devices may be baked for:
- 192 hours at 40°C+5°C/- 0°C and < 5% RH for low temperature device containers, or
- 24 hours at 125°C+5°C/- 0°C for high temperature device containers.

2.2.4 AC Electrical Characteristics and Timing Diagram

2.2.4.1 External Memory Interface for DDR3

The external memory interface shown below is used to connect DDR3 device for MT8516A. It includes pins ED_CLK, ED_CLK_B, RESET_B, ECKE, ECS#, EWR#, ERAS#, ECAS#, EDS[3:0], EDS#[3:0], EA[15:0] and ED[31:0].

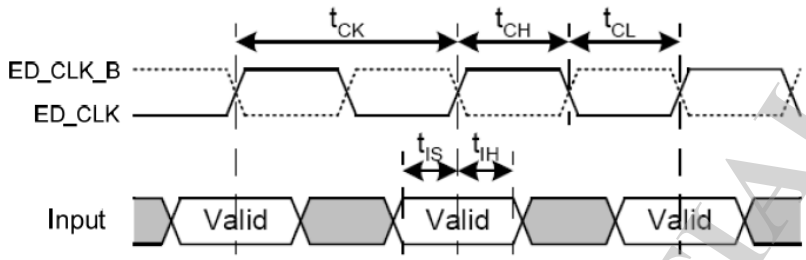


Figure 2-2: Basic timing parameter for DDR3 command

Table 2-19: DDR3 AC timing parameter table of external memory interfaces

Symbol	Description	Min.	Typ.	Max.	Unit
tDQSCK	DQS output access time from CK/CK'	-0.225		0.225	ns
tCK	Clock cycle time	1.25		1.875	ns
tCH	Clock high level width	0.47		0.53	tCK
tCL	Clock low level width	0.47		0.53	tCK
tDS	DQ & DM input setup time	0.01			ns
tDH	DQ & DM input hold time	0.045			ns
tIS	Address & control input setup time	0.045			ns
tIH	Address & control input hold time	0.12			ns
tLZ	DQ & DQS low-impedance time from CK/CK'	-0.45		0.225	ns
tHZ	DQ & DQS high-impedance time from CK/CK'			0.225	ns
tDQSQ	DQS-DQ skew			0.1	ns
tQH	DQ/DQS output hold time from DQS	0.38			tCK
tDQSH	DQS input high-level width	0.45		0.55	tCK
tDQSL	DQS input low-level width	0.45		0.55	tCK
tMRD	MODE register set command period	4			tCK
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	28		9*REFI	tCK
tRC	ACTIVE to ACTIVE command period	36			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	300ns (4gb)			ns
tRCD	ACTIVE to READ or WRITE delay	8			tCK
tRP	PRECHARGE command period	8			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	4			tCK
tWR	WRITE recovery time	6			tCK
tWTR	Internal write to READ command time	6			tCK
tXSDLL	Exit Self Refresh to command requiring a locked DLL	512			tCK
tXPDLL	Exit power down with DLL frozen to commands requiring a locked DLL	20			tCK

Symbol	Description	Min.	Typ.	Max.	Unit
tXP	EXIT power down with DLL to next valid command delay	6			tCK
tCKE	CKE min. pulse width(high & low pulse width)	4			tCK
tREFI	Average periodic refresh interval	3.9			us

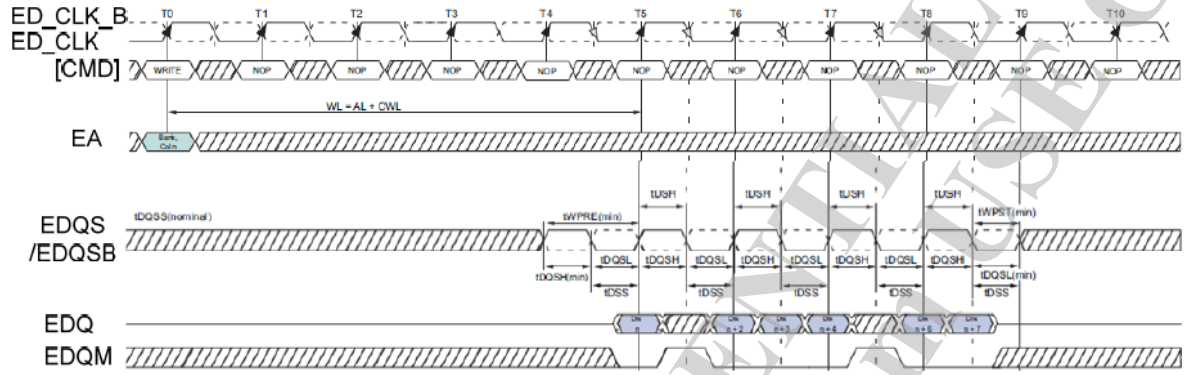


Figure 2-3: Basic Timing Parameter for DDR3 Write

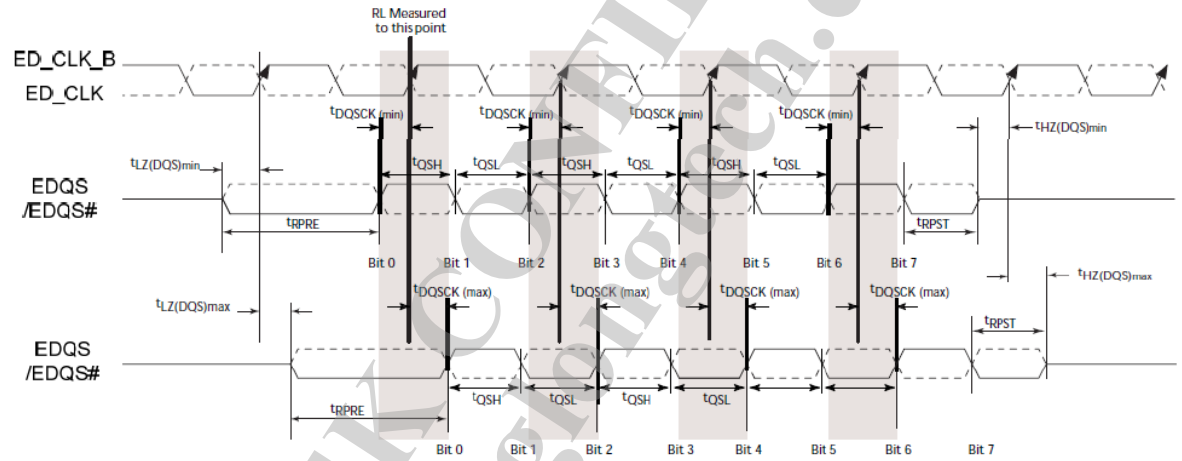
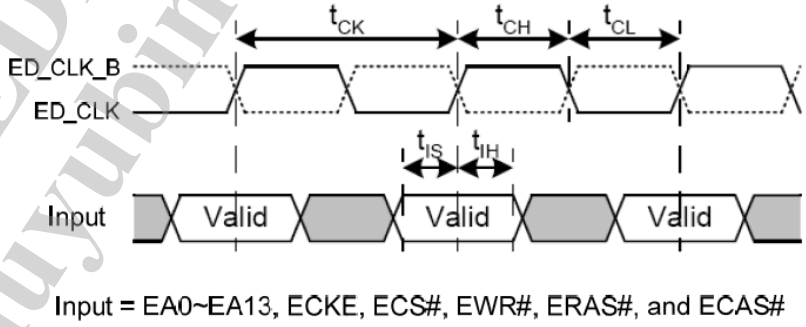


Figure 2-4: Basic Timing Parameter for DDR3 Read

2.2.4.2 External Memory Interface for DDR4

The external memory interface shown below is used to connect DDR4 device for MT8516A. It includes pins ED_CLK, ED_CLK_B, RESET_B, ECKE, EACT, ECS#, EWR#, ERAS#, ECAS#, EDQM[3:0], EDQS[3:0],EDQS#[3:0], EA[13:0] and ED[31:0].

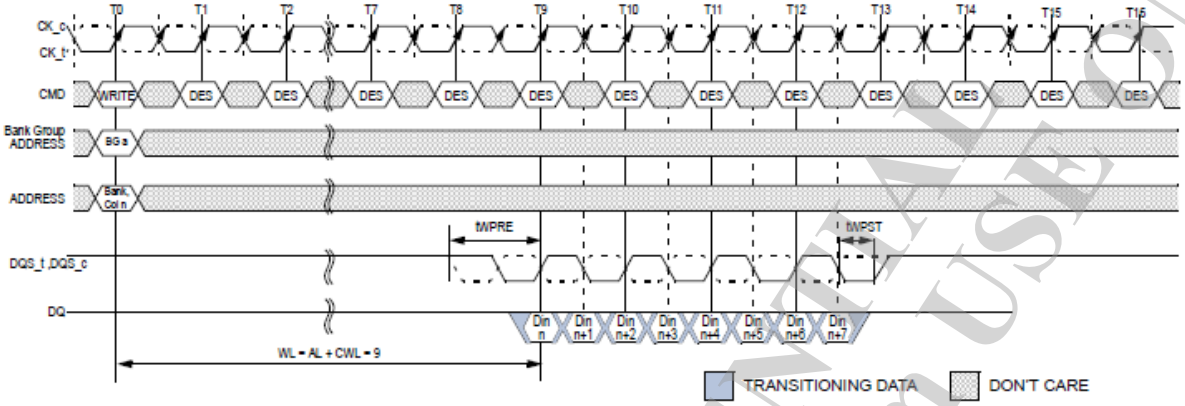


Input = EA0~EA13, ECKE, ECS#, EWR#, ERAS#, and ECAS#

Figure 2-5: Basic timing parameter for DDR4 commands

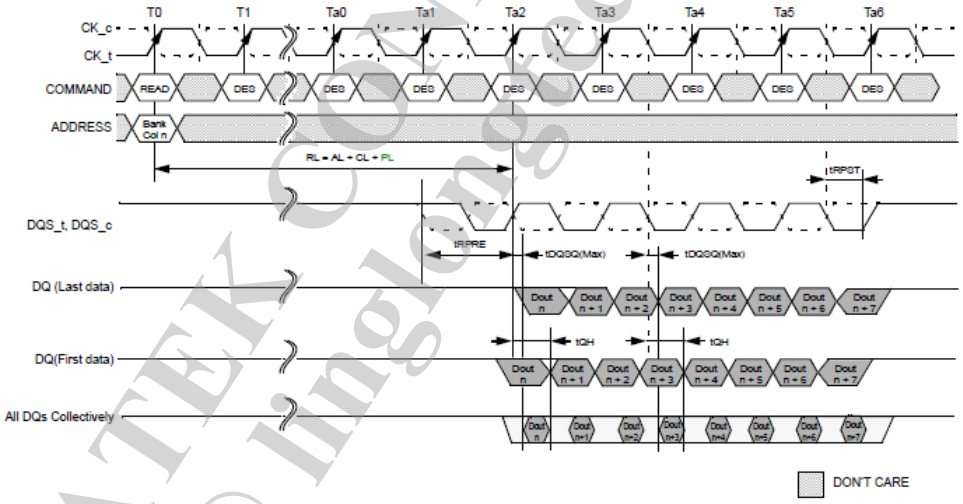
Table 2-20: DDR4 AC timing parameter table of external memory interfaces

Symbol	Description	Min.	Typ.	Max.	Unit
tDQSCK	DQS output access time from CK/CK'	-0.225		0.225	ns
tCK	Clock cycle time	1.25		1.875	ns
tCH	Clock high level width	0.48		0.52	tCK
tCL	Clock low level width	0.48		0.52	tCK
tDS	DQ & DM input setup time	0.1875			ns
tDH	DQ & DM input hold time	0.1875			ns
tIS	Address & control input setup time	0.115			ns
tIH	Address & control input hold time	0.14			ns
tLZ	DQ & DQS low-impedance time from CK/CK'	-0.45		0.225	ns
tHZ	DQ & DQS high-impedance time from CK/CK'			0.225	ns
tDQSQ	DQS-DQ skew			0.16	ns
tQH	DQ/DQS output hold time from DQS	0.74			tCK
tDQSH	DQS input high-level width	0.38		0.62	tCK
tDQSL	DQS input low-level width	0.38		0.62	tCK
tMRD	MODE register set command period	8			tCK
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.33			tCK
tRAS	ACTIVE to PRECHARGE command period	28		9*REFI	tCK
tRC	ACTIVE to ACTIVE command period	38			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	300ns (4gb)			ns
tRCD	ACTIVE to READ or WRITE delay	10			tCK
tRP	PRECHARGE command period	10			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	4			tCK
tWR	WRITE recovery time	6			tCK
tWTR-S	Internal write to READ command time(different bank group)	2			tCK
tWTR-L	Internal write to READ command time(same bank group)	6			tCK
tXSDLL	Exit Self Refresh to command requiring a locked DLL	597			tCK
tXP	EXIT power down with DLL to next valid command delay	6			tCK
tCKE	CKE min. pulse width(high & low pulse width)	4			tCK
tCCD_S	CAS_n-to-CAS_n command delay to different bank group	4			tCK
tCCD_L	CAS_n-to-CAS_n command delay to same bank group	5			tCK
tREFI	Average periodic refresh interval			7.8	us



NOTE :
1. BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 2-6: Basic timing parameter for DDR4 write



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
NOTE 5 Output timings are referenced to VDDQ, and DLL on for locking.
NOTE 6 tDQSQ defines the skew between DQS_t,DQS_c to Data and does not define DQS_t, DQS_c to Clock.
NOTE 7 Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst

Figure 2-7: Basic timing parameter for DDR4 read

2.2.4.3 External Memory Interface for LPDDR2

The external memory interface shown below is used to connect LPDDR2 device for MT8516A. It includes pins ED_CLK, ED_CLK_B, RESET_B, ECKE, ECS#, EDQS[3:0],EDQS#[3:0], EA[9:0] and ED[31:0].

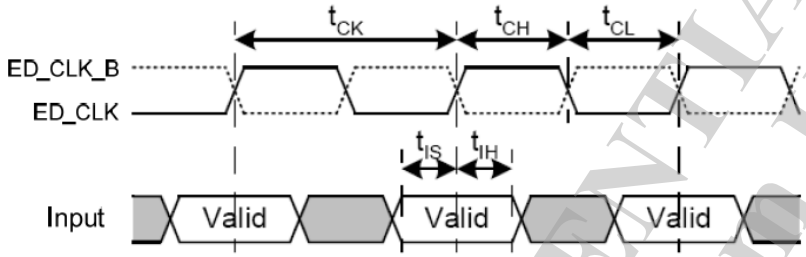


Figure 2-8: Basic timing parameter for LPDDR2 commands

Table 2-21: LPDDR2 AC timing parameter table of external memory interfaces

Symbol	Description	Min.	Typ.	Max.	Unit
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCK	Clock cycle time	1.87		10	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.21			ns
tDH	DQ & DM input hold time	0.21			ns
tIS	Address & control input setup time	0.22			ns
tIH	Address & control input hold time	0.22			ns
tLZ	DQ & DQS low-impedance time from CK/CK'	2.178			ns
tHZ	DQ & DQS high-impedance time from CK/CK'			5.4	ns
tDQSQ	DQS-DQ skew			0.2	ns
tQH	DQ/DQS output hold time from DQS	0.48			tCK
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tMRD	MODE register set command period	5			tCK
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.38			tCK
tRAS	ACTIVE to PRECHARGE command period	23			tCK
tRC	ACTIVE to ACTIVE command period	34			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	70			tCK
tRCD	ACTIVE to READ or WRITE delay	10			tCK
tRP	PRECHARGE command period	10			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	6			tCK
tWR	WRITE recovery time	8			tCK

Symbol	Description	Min.	Typ.	Max.	Unit
tWTR	Internal write to READ command time	4			tCK
tXP	EXIT power down to next valid command delay	4			tCK
tCKE	CKE min. pulse width(high & low pulse width)	3			tCK
tREFI	Average periodic refresh interval	3.9			us

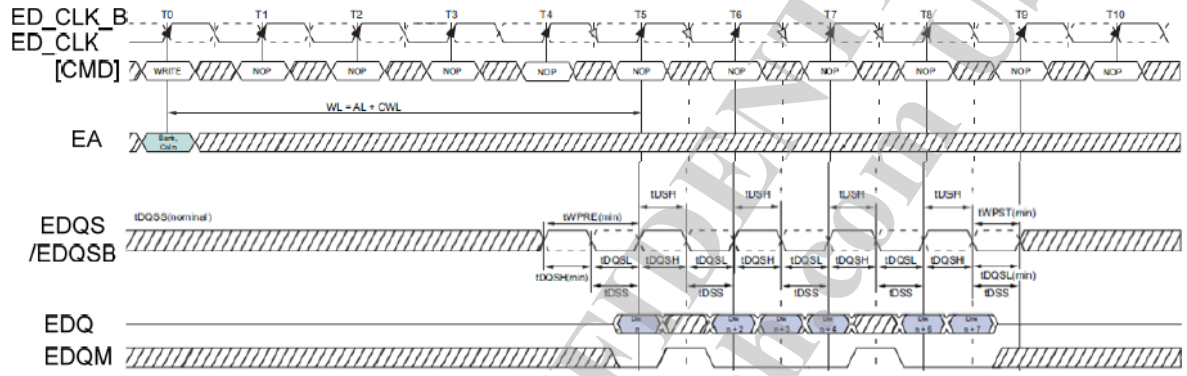


Figure 2-9: Basic timing parameter for LPDDR2 write

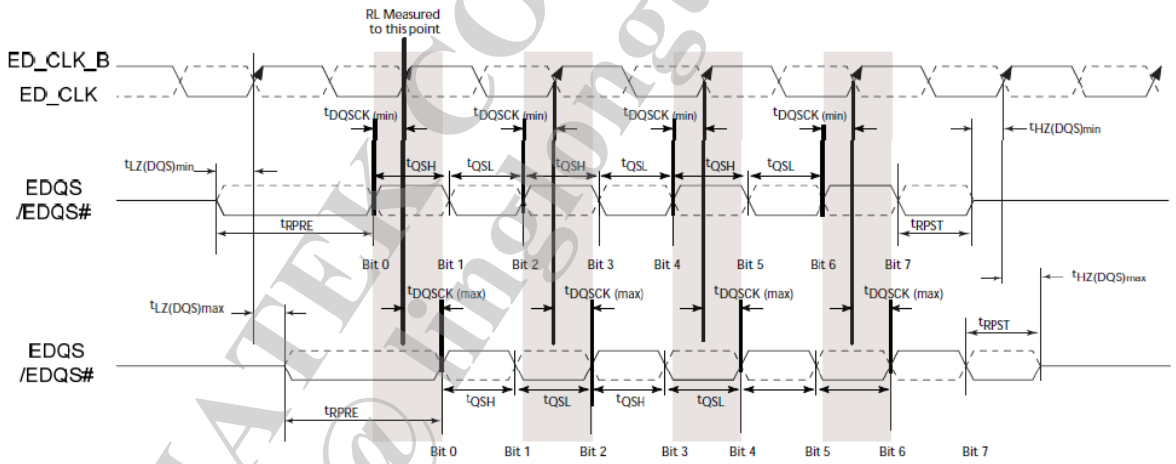


Figure 2-10: Basic timing parameter for LPDDR2 read

2.2.4.4 External Memory Interface for LPDDR3

The external memory interface shown below is used to connect LPDDR3 device for MT8516A. It includes pins ED_CLK, ED_CLK_B, RESET_B, ECKE, ECS#, EDQS[3:0],EDQS#[3:0], EA[9:0] and ED[31:0].

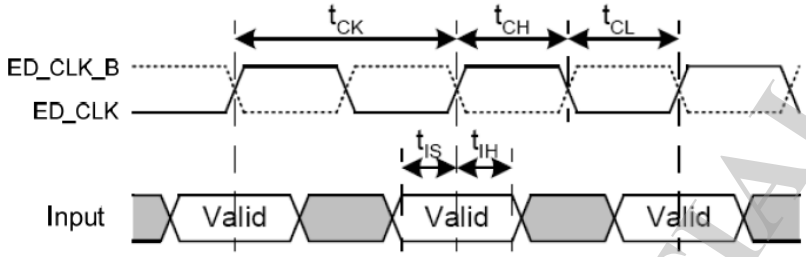


Figure 2-11: Basic timing parameter for LPDDR3 commands

Table 2-22: LPDDR3 AC timing parameter table of external memory interfaces

Symbol	Description	Min.	Typ.	Max.	Unit
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCK	Clock cycle time	1.25		10	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.15			ns
tDH	DQ & DM input hold time	0.15			ns
tIS	Address & control input setup time	0.25			ns
tIH	Address & control input hold time	0.25			ns
tLZ	DQ & DQS low-impedance time from CK/CK'	2.2			ns
tHZ	DQ & DQS high-impedance time from CK/CK'			5.4	ns
tDQSQ	DQS-DQ skew			0.135	ns
tQH	DQ/DQS output hold time from DQS	0.4			tCK
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tMRW	MODE register set command period	10			tCK
tMRR	MODE register set command period	4			tCK
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	18			tCK
tRC	ACTIVE to ACTIVE command period	27			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	84			tCK
tRCD	ACTIVE to READ or WRITE delay	8			tCK
tRP	PRECHARGE command period	10			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	4			tCK
tWR	WRITE recovery time	6			tCK
tWTR	Internal write to READ command time	4			tCK

tXP	EXIT power down to next valid command delay	3			tCK
tCKE	CKE min. pulse width(high & low pulse width)	6			tCK
tREFI	Average periodic refresh interval	3.9			us

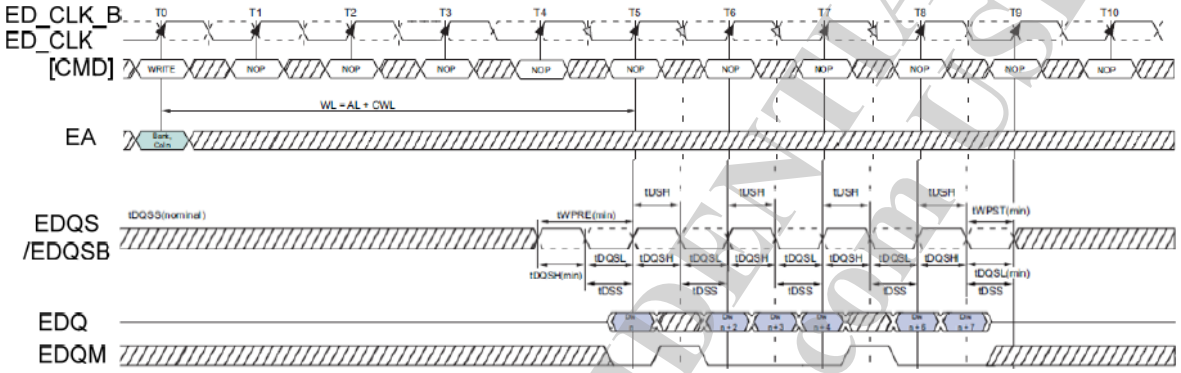


Figure 2-12: Basic timing parameter for LPDDR3 write

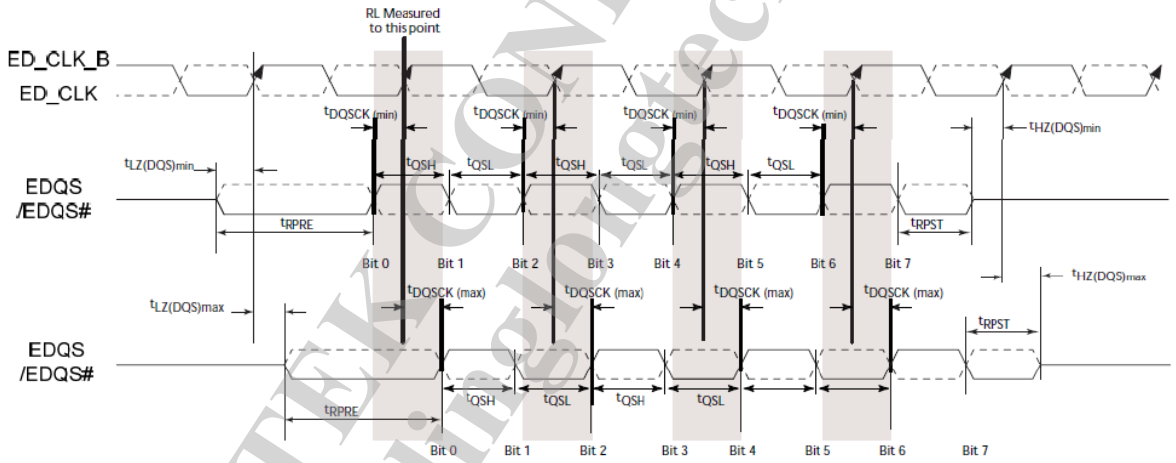


Figure 2-13: Basic timing parameter for LPDDR3 read

Table 2-23: DDR parameter requirements at component pin

Parameter	Comment	Min	Typ	Max	Unit
Per-bit deskew availability		N/A			Y/N
On-Chip dynamic skew span between DQ/DQS	WRITE mode			40	ps
On-Chip dynamic skew span between CMD/CLK				40	ps

Parameter	Comment	Min	Typ	Max	Unit
On-Chip static skew within DQ byte	If per-bit deskew is not available			40	ps
On-Chip static skew within CA bus	If training is not available			40	ps
Max allowed DQ/DQS byte skew span	READ mode, if per-bit deskew is not available			100	ps
Max allowed DQ/DQS single-bit skew span	READ mode, if per-bit deskew is available			165	ps
Required Teye (Aperture-based)	DQ READ, skew between DQ/DQS			120	ps
Required VIH DC/VIL DC			DDR3L: 90 DDR4:75 LP3:100		mV
Required VIH AC/VIL AC			DDR3L: 135 DDR4:100 LP3:150		mV
Max allowed overshoot/undershoot value	See Figure 2-14		DDR3L: 0.4 DDR4:0.3 LP3:0.35		V
Max allowed overshoot/undershoot area	See Figure 2-14		DDR3L: 0.33 DDR4:0.25 LP3:0.1		V*ns

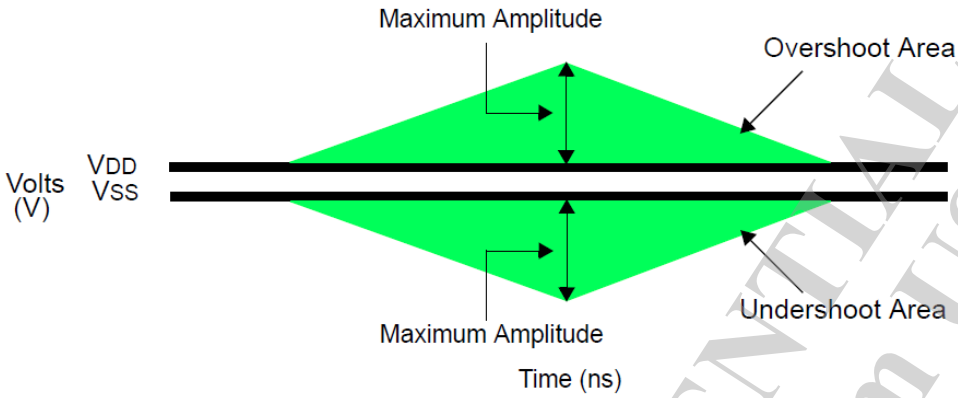


Figure 2-14: Control Overshoot and Undershoot Definition Block

Table 2-24: DDR3 skew tolerances

Length Matching Channel (Board +Package)	Tolerance
Impedance	
DQ-DQS	700 mil
DQ-DQ	700 mil
DQS-CLK	1200 mil
CMD-CLK	200 mil
CMD- CMD (within the same DRAM)	600 mil
CMD- CMD (across DRAMs)	200 mil
CTRL-CLK	200 mil
CTRL-CTRL (within same DRAM)	600 mil
CTRL-CTRL (across DRAMs)	200 mil
CLK-CLK	200 mil

2.2.4.5 I2C Parameter Specification

Table 2-25: I2C parameter specification

Parameter	Description	Min	Typ	Max	Unit
VOL	Output voltage Low	0		0.2VDD①	V
VOH	Output voltage High			1.01VDD	V
Trise	Rise time of SDA and SCL signals	0		120	ns
Tfall	Fall time of SDA and SCL signals	6.5②		120	ns
Thigh	Pulse duration, SCL high			0.26	µs
Tlow	Pulse duration, SCL low			0.5	µs
TSU	Setup time, SDA to SCL	0.05			µs
TST,STA	Setup time, SCL to start condition	0.26			µs
THD,STA	Hold time, start condition to SCL	0.26			µs
TST,STO	Setup time, SCL to stop condition	0.26			µs
T(BUF)	Bus free time between stop and start condition	0.5			µs
Cb③	Capacitive load for each bus line			550	pF

VDD is 1.8V.

For E1: I2C IO can meet spec minimum value: 20 ×(VDD / 5.5 V)=6.5 request，For E2 I2C IO will modify to improve for resistance and C loading range adjustment.

The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application.

2.2.4.6 eMMC Parameter Specification

Table 2-26: eMMC parameter specification

Parameter			Min	Typ	Max	Unit
Clock	Period	HS200	5		-	ns
		DDR50	10		-	ns
		SDR50	20		-	ns
		SDR25	40		-	ns
	Timing	Trise			1.0	ns
		Tfall			1.0	ns
		Duty Cycle	30/45		70/55	%
Timing	HS200	Setup Time	1.4			ns

Parameter			Min	Typ	Max	Unit
		Hold Time	0.8			ns
	SDR25,50	Setup Time	3			ns
		Hold Time	3			ns
Voltage	Supply	I/O Supply	2.5			V
	Input	High	0.9*VCC3IO		VCC3IO+0.3	V
		Low	-0.3		0.1*VCC3IO	V
	Output	High	1.4		VCC3IO+0.3	V
		Low	-0.3		0.35*VCC3IO	V

2.2.4.7 SD Parameter Specification

Table 2-27: SD parameter specification

Parameter			Min	Typ	Max	Unit
Clock	Period	SDR104	4.8			ns
		SDR50	10			ns
		SDR25	20			ns
		SDR12	38			ns
	Timing	Trise	-		0.96	ns
		Tfall	-		0.96	ns
		Duty Cycle	30		70	%
Timing	SDR104	Setup Time	1.4		-	ns
		Hold Time	0.8		-	ns
	SDR12,25,50	Setup Time	3.0		-	ns
		Hold Time	0.8		-	ns
Voltage	Supply	I/O Supply				V
	Input	High	1.27		VCC3IO+03	V
		Low	-0.3		0.58	V
	Output	High	1.4		VCC3IO+03	V

Parameter			Min	Typ	Max	Unit
		Low	-0.3		0.45	V

2.3 System Configuration

2.3.1 Constant Tie Pins

Table 2-28: Constant tied pins of MT8516A

Pin name	Description
TESTMODE	Test mode (tie to GND)
FSOURCE_P	EFUSE blowing (tie to GND)

2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

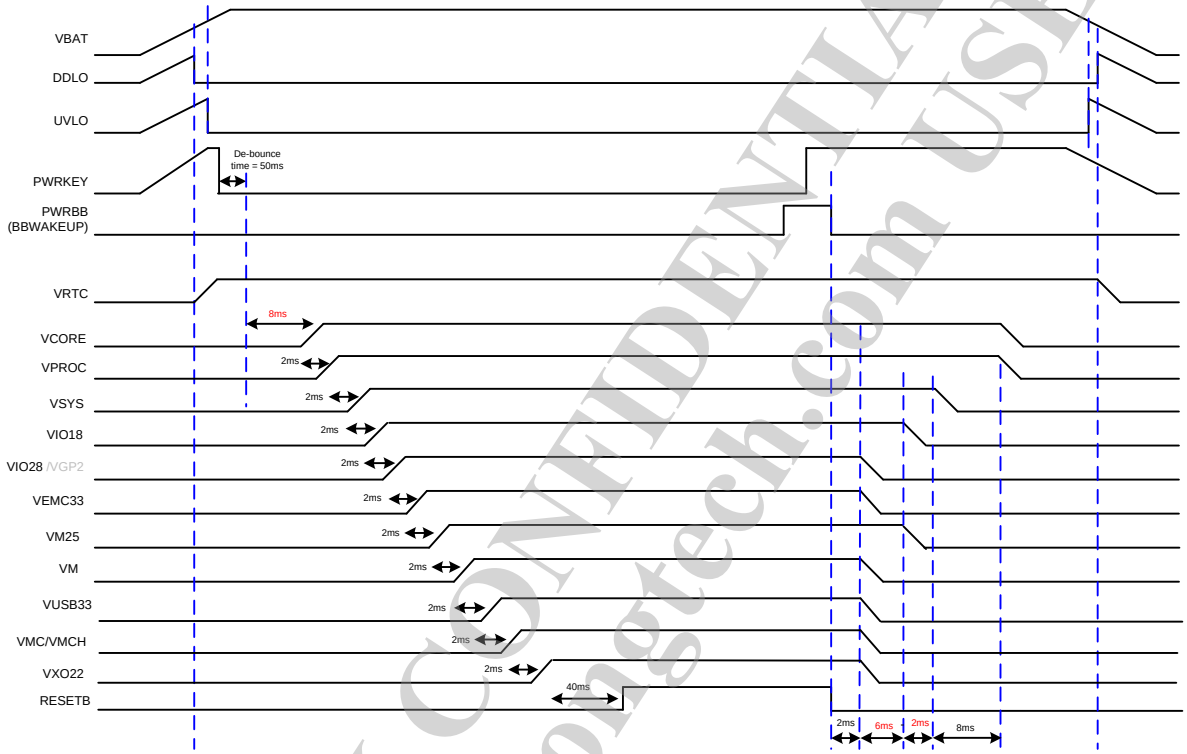


Figure 2-15: Power on/off sequence with XTAL

Figure below shows the power-on/off sequence without XTAL. VXO22 is always turned on when VBAT is above the DDLO threshold.

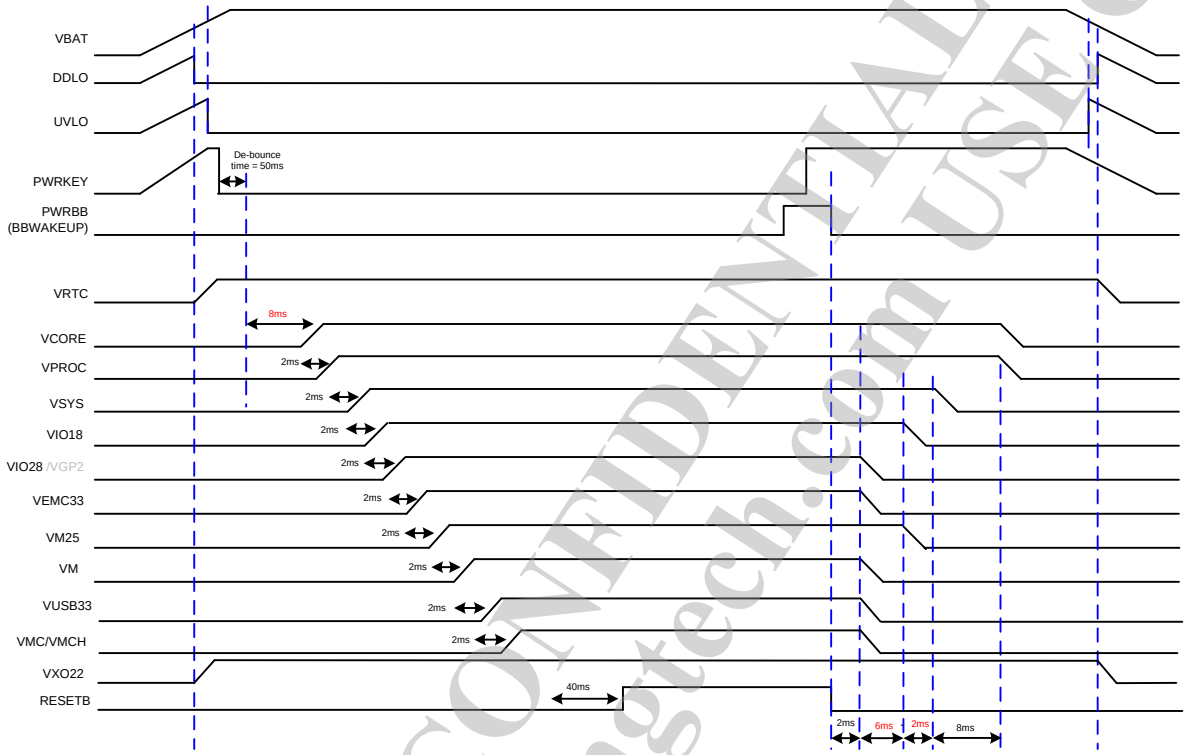


Figure 2-16: Power on/off sequence without XTAL

2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete application processor:

- Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
- Clock generation: PLLs providing clock signals to MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete application processor:

- AUXADC
- Phase locked loop
- Temperature sensor
- AUDIO CODEC

2.5.3 Block Diagram

2.5.3.1 AUXADC

2.5.3.1.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measuring and some for external voltage measuring. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

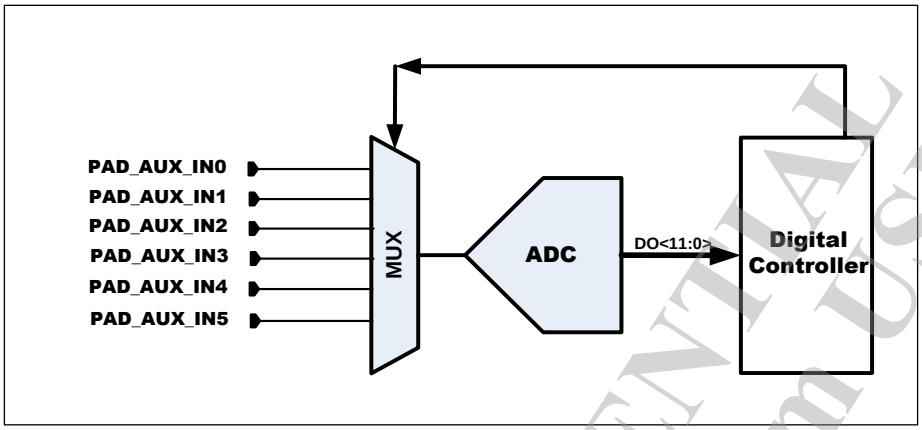


Figure 2-17: AUXADC Block Diagram

Table 2-29: Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	NA
Channel 3	NA
Channel 4	NA
Channel 5	Internal use(AUDIO)
Channel 6	Internal use(AUDIO)
Channel 7	Internal use(AUDIO)
Channel 8	Internal use(AUDIO)
Channel 9	External use (AUX_IN2)
Channel 10	Internal use(Thermal Sensor)
Channel 11	Internal use(Thermal Sensor)
Channel 12	External use (AUX_IN3)
Channel 13	External use (AUX_IN4)
Channel 14	External use (AUX_IN5)
Channel 15	Internal use(ACC_DET)

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-30: AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0		1.5	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
CIN	Input capacitance Unselected channel Selected channel		 50 4		 fF pF
RIN	Input resistance Unselected channel	400			MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
SINAD	Signal to noise and distortion ratio (1kHz full swing input & 1.0833MHz clock rate)	62	68		dB
DVDD	Digital power supply	0.945	1.15	1.31	V
AVDD	Analog power supply	1.7	1.8	1.9	V
	Current consumption Power-up Power-down		 535 15		 uA uA

2.5.3.2 Phase Locked Loop

2.5.3.2.1 Block Descriptions

There are total 8 PLLs in PLL macro, providing several clocks for CPU, BUS, MSDC and image-sensor.

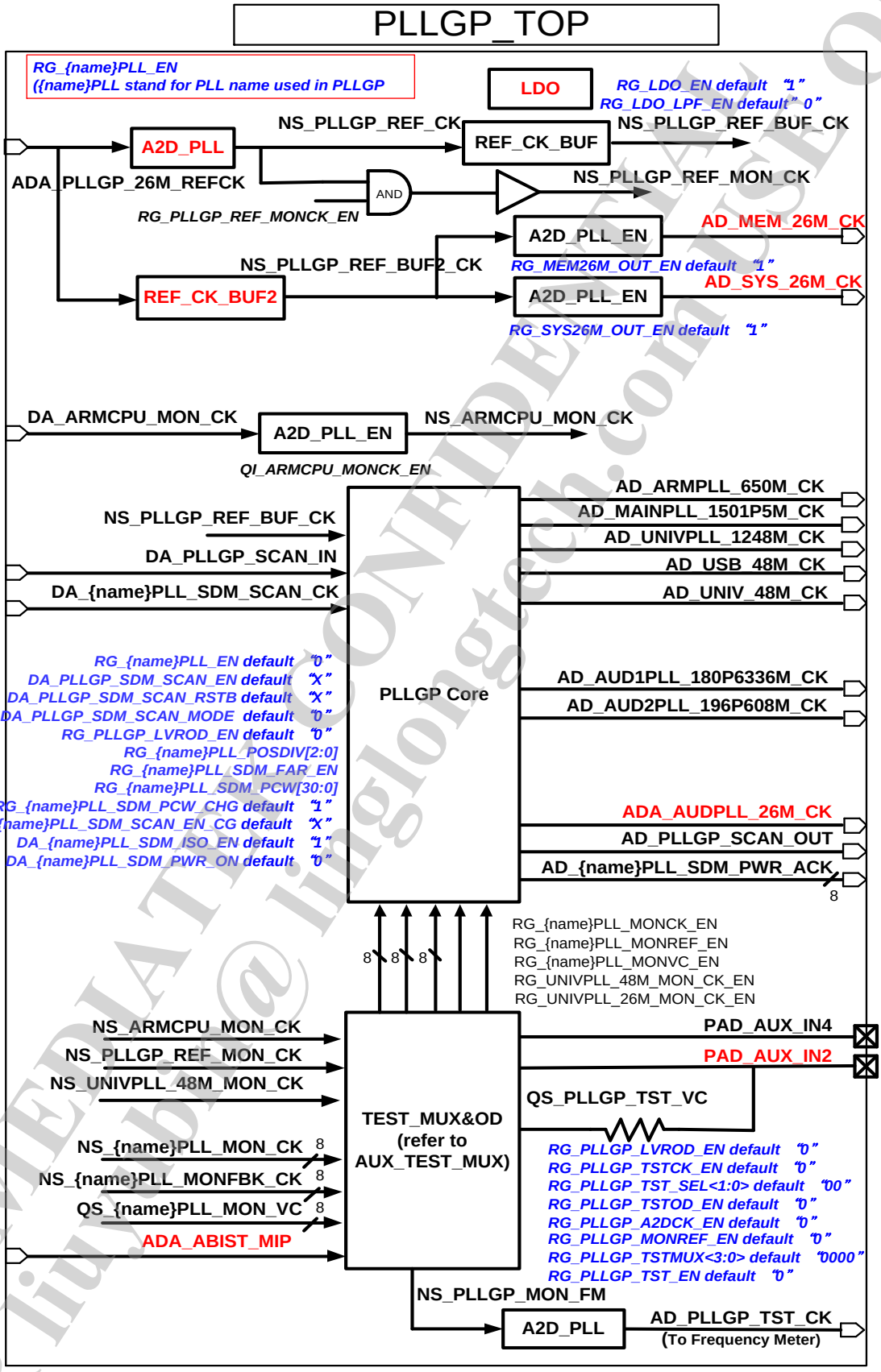


Figure 2-18: PLL Block Diagram

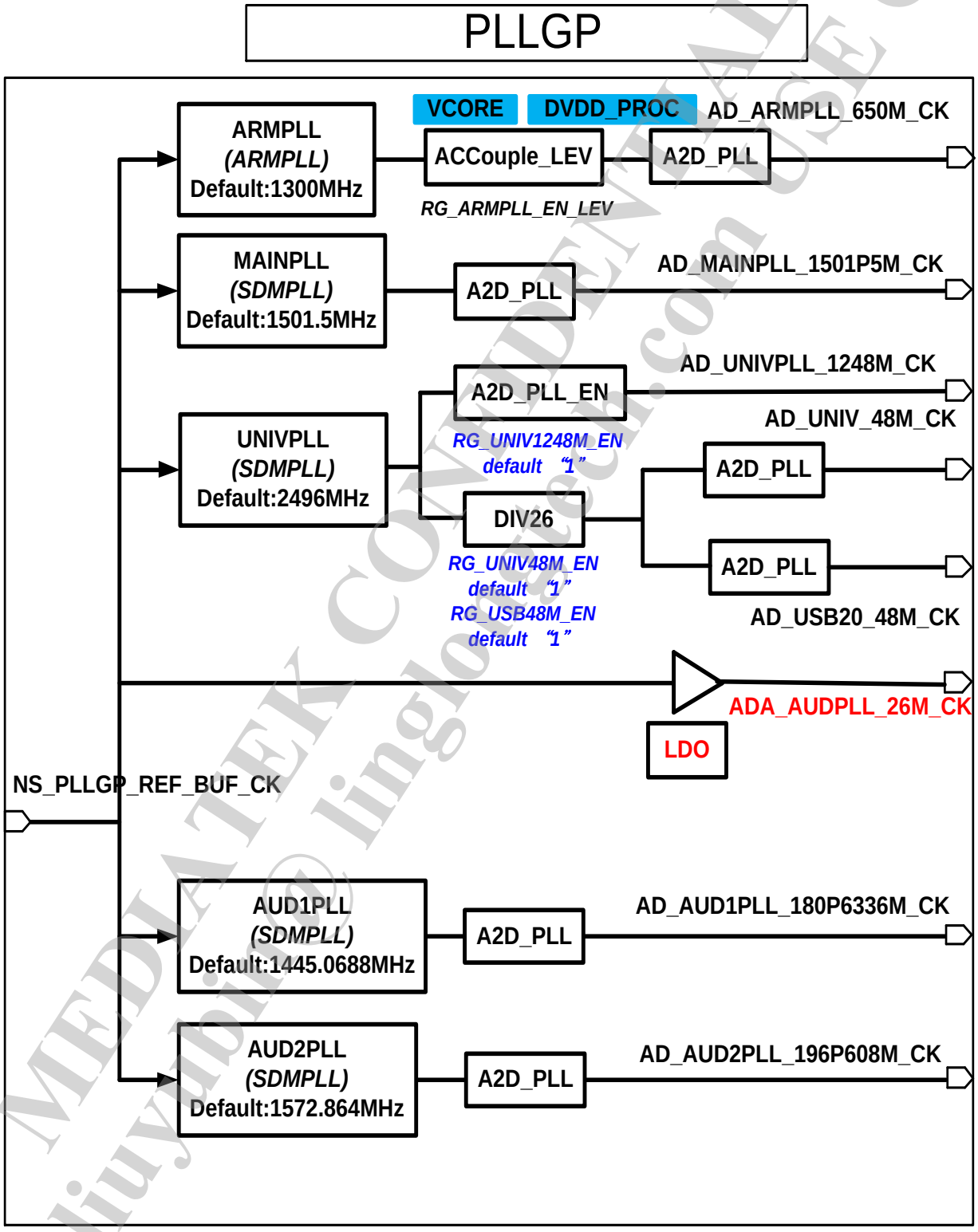


Figure 2-19: PLL Core Block Diagram

2.5.3.2.2 Functional Specifications

See the table below for the functional specifications of PLL.

Table 2-31: 26M Reference specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		26(System) 26(MEM) 26(AUDPLL)		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.15	1.31	V
AVDD	Analog power supply	1.7	1.8	1.9	V
	Current consumption		1.2		mA
	Power-down current consumption			12	uA

Table 2-32: ARMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		650		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.15	1.31	V
AVDD	Analog power supply	1.7	1.8	1.9	V
	Current consumption		1.2		mA
	Power-down current consumption			12	uA

Table 2-33: MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1501.5		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.15	1.31	V
AVDD	Analog power supply	1.7	1.8	1.9	V
	Current consumption		1.2		mA
	Power-down current consumption			12	uA

Table 2-34: UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	1248 48(USB) 48(UNIV)	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		< 30ps P-P for 1248M < 60ps P-P for 48M		ps
DVDD	Digital power supply	0.945	1.15	1.31	V
AVDD	Analog power supply	1.7	1.8	1.9	V
	Current consumption		0.8		mA
	Power-down current consumption			12	uA

Table 2-35: AUD1PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		180.6336		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		100		ps
DVDD	Digital power supply	0.945	1.15	1.31	V
AVDD	Analog power supply	1.7	1.8	1.9	V
	Current consumption		1.2		mA
	Power-down current consumption			12	uA

Table 2-36: AUD2PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		196.608		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		100		ps
DVDD	Digital power supply	0.945	1.15	1.31	V
AVDD	Analog power supply	1.7	1.8	1.9	V
	Current consumption		1.2		mA
	Power-down current consumption			12	uA

2.5.3.3 Temperature Sensor

2.5.3.3.1 Block Descriptions

Several temperature sensors are provided to monitor the temperature of CPUs. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.3.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-37: Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		105	°C
	Accuracy	-7		7	°C
	Active current		300		uA
	Quiescent current		3		uA

2.5.3.4 AUDIO CODEC

2.5.3.4.1 Block Descriptions

The audio uplink path is composed of PGA and audio ADC. There are three input pairs of the uplink path to support dual-MIC, earphone-MIC and digital MIC. The audio downlink is composed of stereo audio DACs, stereo headphone drivers and lineout driver. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec. The Audio Downlink includes the following blocks: DAC and headphone driver, there are 2 Channels to support stereo headphone; and a voice amplifier lineout to drive off-chip speaker amplifier.

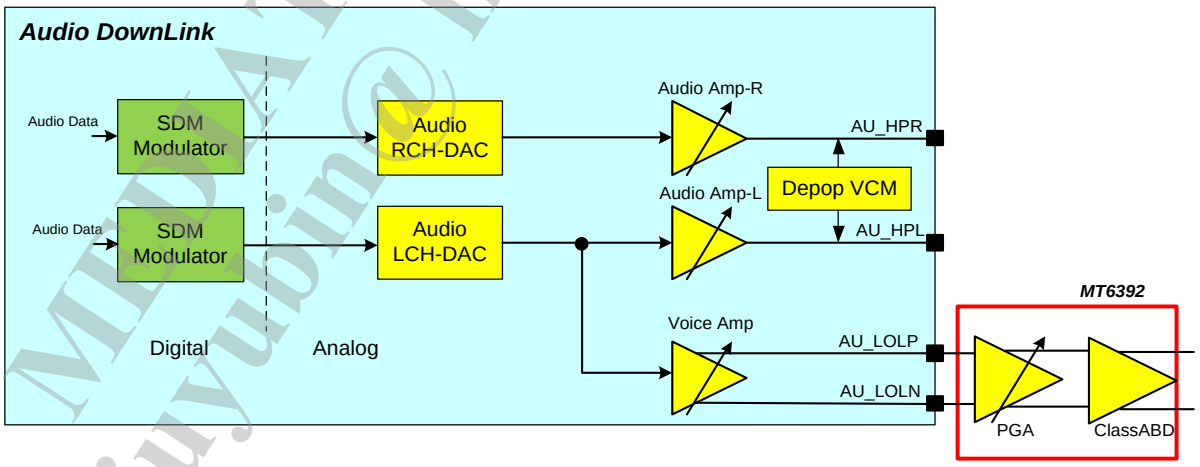


Figure 2-20: Audio Downlink Block Diagram

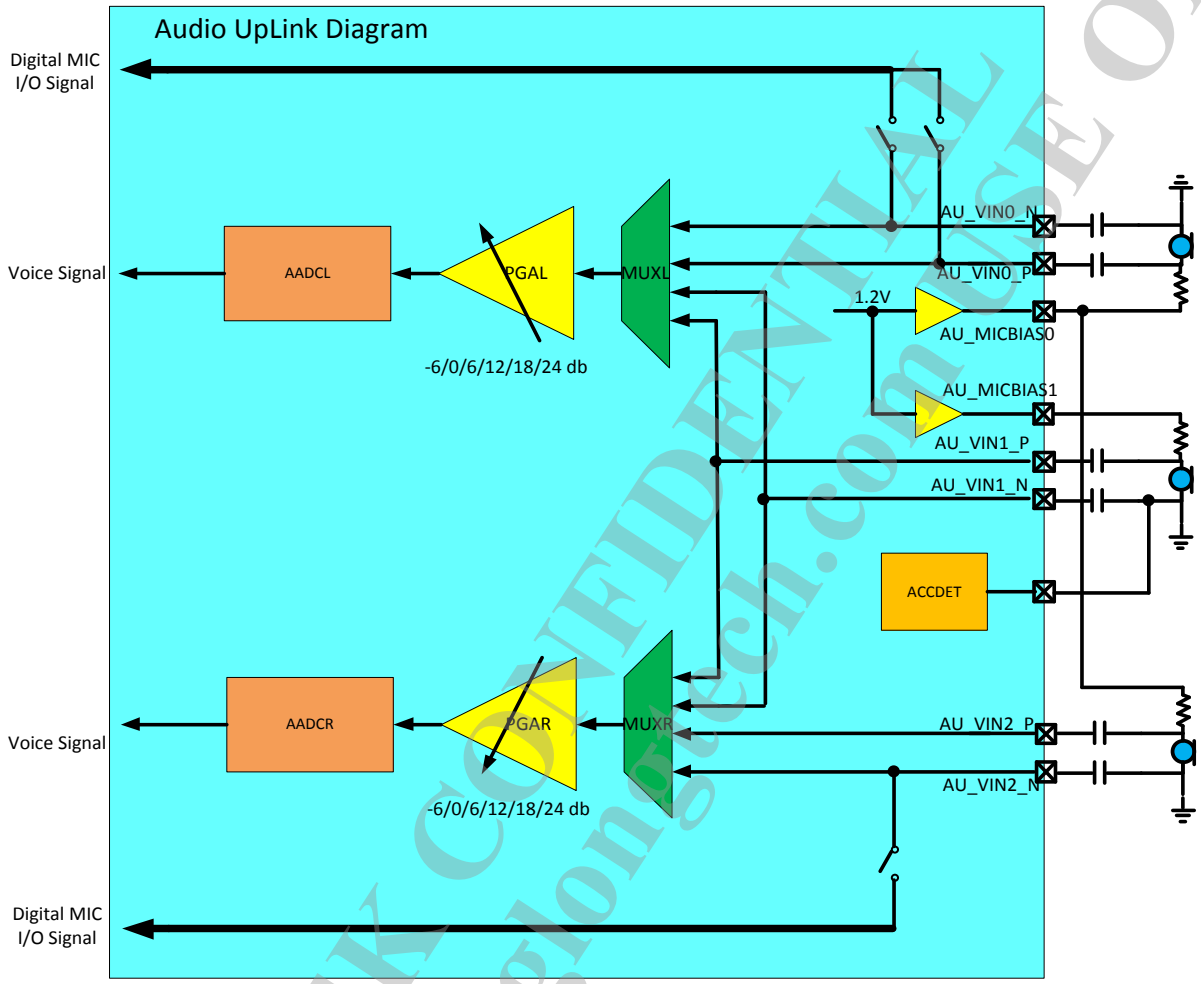


Figure 2-21: Audio Uplink Block Diagram

2.5.3.4.2 Functional Specifications

The analog blocks include the following analog functions for complete application processor:

- Audio Downlink
- stereo headphone drivers
- Lineout driver
- Audio Uplink
- Dual MIC/earphone MIC/digital MIC
- multi-key accessory detection
- MIC bias voltages

Table 2-38: Audio Downlink and Uplink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	2.8V Analog Power(V28)	2.7	2.8	2.9	V
	2.2V Analog Power(V22)	2.1	2.2	2.3	V
	Digital Power Supply(V10)	0.945	1.15	1.31	V
AUDIO DownLink, AUDIOLINK SPEC					
	Clock Frequency (FCK)		6.5		MHz
	Sample Rate (Fs)	32	44.1	48	KHz
	Current Consumption (IDC)		11		mA
	Peak Signal to Noise Ratio (PSNR) HP AMP Gain=0dB; @All zeros fed to DAC Input		90		dB
	Dynamic Range (DR) HP AMP Gain=0dB; @-60dBFS Input		90		dB
	Output Swing for 0dBFS Input Level			0.85	Vrms
	Total Harmonic Distortion (THD) Plus Noise 11 mW@ 0dBFS, 64Ω		-83	-70	dB
	Output Resistor Load(Single-ended)	64	132		Ohm
	Output Capacitor Load			250	pF
	L-R Channel Crosstalk (XT)		92		dB
AUDIO DownLink, VoiceLINK SPEC					
	Peak Signal to Noise Ratio (PSNR) Lineout Amp Gain=4dB; @All zeros fed to DAC Input		91		dB
	Dynamic Range (DR) Lineout Amp Gain=4dB; @-60dBFS Input		91		dB
	Output Swing for 0dBFS Input Level			1.273	Vrms
	THD+N Total Harmonic Distortion Plus Noise @ 0dBFS,12KΩ		-83		dB
	Output Resistor Load(Differential)	12			Ohm
	Peak Signal to Noise Ratio (PSNR) Lineout Amp Gain=4dB; @All zeros fed to DAC Input		91		dB
Analog Uplink MIC Path					
	Current Consumption (1 channel)		2		mA
	Total Harmonic Distrotion+Noise(THD+N) Input Level : -60dBm0(PGA gain=0dB) Input Level : 0dBm0(PGA gain=0dB)		 -25 -82		 dB dB
	Input Impedance(Differential)	13	20	27	KOhm
	L-R Channel Crosstalk(XT)		95		dB

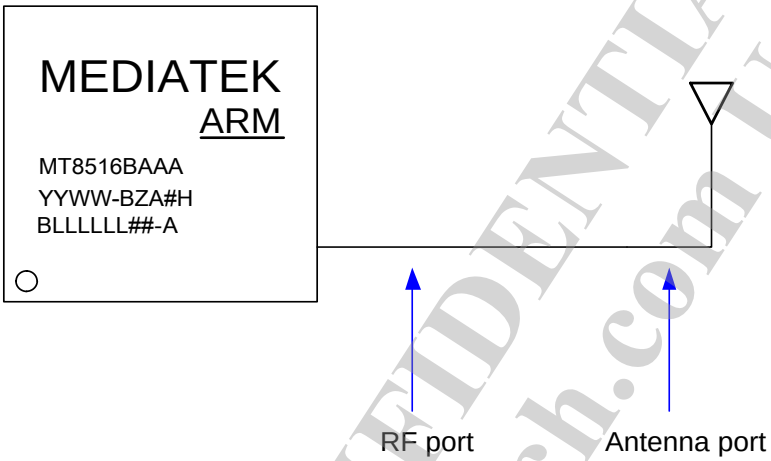
Digital MIC Path					
	DMIC Clock Frequency		1.625/3.25		MHz
	DMIC Clock Duty Cycle	40		60	%
	DMIC Clock Rise time(Max CL=80p)		10		ns
	DMIC Clock Fall time(Max CL=80p)		10		ns
	Sample Rate(FS)	8	16	32/48	KHz
Audio Uplink MICBIAS					
	Microphone0 Biasing Voltage	1.9		2.2	V
	Microphone1 Biasing Voltage	1.9		2.5	V
	Current draw from microphone bias		2		mA

For DMIC 48K Hz: Must use 3.25M DMIC clock PDM to PCM conversion swing limitation at 48K mode, When digital swing < -12dBFS, PDM to PCM conversion output would be boosted 12dB When PCM's digital swing >= -12dBFS, it will cause saturation in recorded PCM data

Frequency response passband ripple (only for digital filter) 0~20K : 2dB， 0~8K : 0.4dB

2.6 Connectivity RF Characteristic

The WLAN radio characteristics are described in this section where the RF port and antenna port of MT8516A can be directly connected by a 50Ohm trace.



2.6.1 Wi-Fi RF Radio Characteristic

The WLAN radio characteristics are described in this section. Unless otherwise specified, all specifications are measured at the chip output RF port.

2.6.1.1 Wi-Fi Receiver Specification

Note: The specification value is valid at room temperature (25oC).

Table 2-39: 2.4GHz receiver specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,412	-	2,484	MHz
RX sensitivity [a]	1 Mbps DSSS		-95		dBm
	2 Mbps DSSS		-93		dBm
	5.5 Mbps DSSS		-91		dBm
	11 Mbps DSSS		-88		dBm
RX Sensitivity [a]	6 Mbps OFDM		-91.5		dBm
	9 Mbps OFDM		-90		dBm
	12 Mbps OFDM		-89		dBm
	18 Mbps OFDM		-86.5		dBm
	24 Mbps OFDM		-83.5		dBm
	36 Mbps OFDM		-80		dBm
	48 Mbps OFDM		-76		dBm
	54 Mbps OFDM		-74.5		dBm
RX sensitivity [b]	MCS 0		-91.5		dBm
BW = 20MHz	MCS 1		-88		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
Green field	MCS 2		-86		dBm
800nS guard interval	MCS 3		-83		dBm
Non-STBC	MCS 4		80		dBm
	MCS 5		-75.5		dBm
	MCS 6		-74		dBm
	MCS 7		-72.5		dBm
RX sensitivity	MCS 0		-88.5		dBm
BW = 40MHz	MCS 1		-85		dBm
Green field	MCS 2		-83		dBm
800nS guard interval	MCS 3		-80		dBm
Non-STBC	MCS 4		-77		dBm
	MCS 5		-72.5		dBm
	MCS 6		-71		dBm
	MCS 7		-69		dBm
Maximum receive level	11 Mbps DSSS			-5	dBm
	6 Mbps OFDM			-10	dBm
	54 Mbps OFDM			-10	dBm
	MCS0			-10	dBm
	MCS7			-10	dBm
Adjacent channel rejection (30MHz offset)	1 Mbps DSSS			40	dB
Adjacent channel rejection (25MHz offset)	11 Mbps DSSS			40	dB
Adjacent channel rejection (25MHz offset)	6 Mbps OFDM			34	dB
	54 Mbps OFDM			22	dB
Adjacent channel rejection (25MHz offset), BW = 20MHz	MCS 0			25	dB
	MCS 7			5	dB
Adjacent channel rejection (40MHz offset), BW = 40MHz	MCS 0			26	dB
	MCS 7			1	dB
Blocking level for 1dB RX sensitivity degradation	776 ~ 794 MHz CDMA2000				dBm
	824 ~ 849 MHz GSM				dBm
	880 ~ 915 MHz GSM				dBm
	1,710 ~ 1,785 MHz GSM				dBm
	1,850 ~ 1,910 MHz GSM				dBm
	1,850 ~ 1,910 MHz WCDMA				dBm
	1,920 ~ 1,980 MHz WCDMA				dBm

a: Degraded by 1.5dB at 85oC
b: Sensitivity degradation in different MCS modes: mixed-mode normal GI: 1dB, mixed-mode short GI: 1dB, and STBC:1dB

2.6.1.2 Wi-Fi Transmitter Specification

Note:

The specification value is valid at room temperature (25oC).
All specifications are measured at the RF port unless otherwise specified.
Typical output power degradation around 3dB at FCC band edge channels

Table 2-40: 2.4GHz transmitter specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,412	-	2,484	MHz
Output power	802.11b, 1~11 Mbps DSSS		19		dBm
VCN35=3.5V	802.11g, 6 ~36Mbps OFDM		16.5		dBm
	802.11g, 48 ~54Mbps OFDM		16		dBm
	802.11n, HT20 MCS0~4		16.5		dBm
	802.11n, HT20 MCS5~7		15.5		dBm
	802.11n, HT40 MCS0~4		15.5		dBm
	802.11n, HT40 MCS5~7		14		dBm
EVM	802.11b, 1~11 Mbps DSSS @Pout=19dBm		25		%
	802.11g, 6 ~36Mbps OFDM@Pout=16.5dBm			-19	dB
	802.11g, 48 ~54Mbps OFDM@Pout=16dBm		-28		dB
	802.11n, HT20 MCS0~4@Pout=16.5dBm			-19	dB
	802.11n, HT20 MCS5~7@Pout=15.5dBm		-28		dB
	802.11n, HT40 MCS0~4@Pout=15.5dBm			-19	dB
	802.11n, HT40 MCS5~7@Pout=14dBm		-30		dB
TX power accuracy	-20~65 oC,5~22dBm			±1.5	dB
Loadpull variation at VSWR = 2:1	Output power variation			±1.5	dB
	EVM degradation		4		dB
Transmitted power (Data rate = 6M, Pout = 17dBm)	76 ~ 108 MHz		-142		dBm/Hz
	776 ~ 794 MHz		-142		dBm/Hz
	869 ~ 960 MHz		-142		dBm/Hz
	925 ~ 960 MHz		-142		dBm/Hz
	1,570 ~ 1,580 MHz		-140		dBm/Hz
	1,805 ~ 1,880 MHz		-131		dBm/Hz
	1,930 ~ 1,990 MHz		-126		dBm/Hz
	2,110 ~ 2,170MHz		-125		dBm/Hz
Harmonic output power (Data rate = 1M, Pout = 19dBm) i	2nd harmonic			-43	dBm/MHz
	3rd harmonic			-43	dBm/MHz

2.6.2 Bluetooth RF Radio Characteristics

2.6.2.1 Basic Data Rate Receiver Specification

Table 2-41: Basic data rate receiver specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402		2,480	MHz
Receiver sensitivity	BER < 0.1%		-92		dBm
Max. usable signal	BER < 0.1%	-20	-5		dBm
C/I co-channel	Co-channel selectivity (BER < 0.1%)	-	6	11	dB
C/I 1MHz	Adjacent channel selectivity (BER < 0.1%)	-	-7	0	dB
C/I 2MHz	2nd adjacent channel selectivity (BER < 0.1%)	-	-39	-30	dB
C/I ≧3MHz	3rd adjacent channel selectivity (BER < 0.1%)	-	-43	-40	dB
C/I image channel	Image channel selectivity (BER < 0.1%)	-	-20	-9	dB
C/I image 1MHz	1MHz adjacent to image channel selectivity (BER < 0.1%)	-	-35	-20	dB
Out-of-band blocking*	30MHz to 2,000MHz	-10			dBm
	2,001MHz to 2,339MHz	-27			dBm
	2,501MHz to 3,000MHz	-27			dBm
	3,001MHz to 12.75GHz	-10			dBm
Intermodulation	Max. interference level to maintain 0.1% BER	-39			dBm

2.6.2.2 Basic Data Rate Transmitter Specification

Table 2-42: Basic data rate transmitter specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Output power	At max power output level		6		dBm
Power control step		2	4	8	dB
ICFT	Initial carrier frequency drift	-75	±18	75	kHz
Carrier frequency drift	One slot packet (DH1)	-25	±15	25	kHz
	Three slot packet (DH3)	-40	±15	40	kHz
	Five slot packet (DH5)	-40	±15	40	kHz
	Max. drift rate	-20	10	20	kHz/50us
Modulation characteristic	$\Delta f1_{avg}$	140	157	175	kHz
	$\triangle f2_{max}$ (for at least 99% of all $\Delta f2_{max}$)	115	145	-	kHz
	$\triangle f2_{avg}/\Delta f1_{avg}$	0.8	0.98	-	
20-dB bandwidth		-	922	1,000	kHz
In-band spurious emission	±2MHz offset		-38	-20	dBm
	±3MHz offset		-43	-40	dBm
	>±3MHz offset		-43		dBm

Parameter	Description	Min.	Typ.	Max.	Unit
Out-of-band spurious emission**	30MHz to 1GHz			-36	dBm
	1GHz to 12.75GHz			-30	dBm
	1.8GHz to 1.9GHz			-47	dBm
	5.15 to 5.3GHz			-47	dBm

2.6.2.3 Enhanced Data Rate Receiver Specification

Table 2-43: Enhanced data rate receiver specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	π/4 DQPSK (BER < 0.01%)	-	-91	-70	dBm
	8PSK (BER < 0.01%)	-	-85.5	-70	dBm
Max. usable signal	π/4 DQPSK (BER < 0.1%)	-20	-5	-	dBm
	8PSK (BER < 0.1%)	-20	-5	-	dBm
C/I co-channel	π/4 DQPSK (BER < 0.1%)	-	9	13	dB
	8PSK (BER < 0.1%)	-	16	21	dB
C/I 1MHz	π/4 DQPSK (BER < 0.1%)	-	-12	0	dB
	8PSK (BER < 0.1%)	-	-6	5	dB
C/I 2MHz	π/4 DQPSK (BER < 0.1%)	-	-36	-30	dB
	8PSK (BER < 0.1%)	-	-33	-25	dB
C/I ≧3MHz	π/4 DQPSK (BER < 0.1%)	-	-43	-40	dB
	8PSK (BER < 0.1%)	-	-40	-33	dB
C/I image channel	π/4 DQPSK (BER < 0.1%)	-	-20	-7	dB
	8PSK (BER < 0.1%)	-	-15	0	dB
C/I image 1MHz	π/4 DQPSK (BER < 0.1%)	-	-40	-20	dB
	8PSK (BER < 0.1%)	-	-30	-13	dB

2.6.2.4 Enhanced Data Rate Transmitter Specification

Table 2-44: Enhanced data rate transmitter specification

Parameter	Description		Min.	Typ.	Max.	Unit
Frequency range			2,402		2,480	MHz
Output power	π/4 DQPSK			3		dBm
	8PSK			3		dBm
Relative transmit power	π/4 DQPSK		-4	-1.7	1	dB
	8PSK		-4	-1.7	1	dB
Frequency stability	ω_o	π/4 DQPSK	-10	±4	10	kHz
		8PSK	-10	±4	10	kHz
	ω_i	π/4 DQPSK	-75	±20	75	kHz
		8PSK	-75	±20	75	kHz
	$\lvert\omega_o+\omega_i\rvert$	π/4 DQPSK	-75	±20	75	kHz
		8PSK	-75	±20	75	kHz

Parameter	Description		Min.	Typ.	Max.	Unit
Modulation accuracy	RMS DEVM	π/4 DQPSK	-	8	20	%
		8PSK	-	8	13	%
	99% DEVM	π/4 DQPSK	-	12	30	%
		8PSK	-	12	20	%
	Peak DEVM	π/4 DQPSK	-	17	35	%
		8PSK	-	17	25	%
In-band spurious emission	±1MHz offset	π/4 DQPSK		-29	-26	dB
		8PSK		-29	-26	dB
	±2MHz offset	π/4 DQPSK		-23	-20	dBm
		8PSK		-23	-20	dBm
	±3MHz offset	π/4 DQPSK		-42	-40	dBm
		8PSK		-42	-40	dBm

2.6.2.5 LE Receiver Specification

Table 2-45: Bluetooth LE receiver specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402		2,480	MHz
Receiver sensitivity (*)	PER < 30.8%		-95	-70	dBm
Max. usable signal	PER < 30.8%	-20	-5		dBm
C/I co-channel	Co-channel selectivity (PER < 30.8%)		6	21	dB
C/I 1MHz	Adjacent channel selectivity (PER < 30.8%)		-7	15	dB
C/I 2MHz	2nd adjacent channel selectivity (PER < 30.8%)		-30	-17	dB
C/I ≧3MHz	3rd adjacent channel selectivity (PER < 30.8%)		-33	-27	dB
C/I Image channel	Image channel selectivity (PER < 30.8%)		-20	-9	dB
C/I Image 1MHz	1MHz adjacent to image channel selectivity (PER < 30.8%)		-30	-15	dB
Out-of-band blocking	30MHz to 2,000MHz	-30			dBm
	2,001MHz to 2,339MHz	-35			dBm
	2,501MHz to 3,000MHz	-35			dBm
	3,001MHz to 12.75GHz	-30			dBm

2.6.2.6 LE Transmitter Specification

Table 2-46: Bluetooth LE transmitter specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Output power(*)	At max. power output level	-20	6	10	dBm
Carrier frequency offset and drift	Frequency offset	-150	±10	150	kHz
	Frequency drift	-50	±10	50	kHz
	Max. drift rate	-20	±10	20	kHz/50us
Modulation characteristic	$\Delta f1_{avg}$	225	251	275	kHz
	$\Delta f2_{max}$ (For at least 99% of all $\Delta f2_{max}$)	185	215		kHz
	$\Delta f2_{avg}/\Delta f1_{avg}$	0.8	0.88		
In-band spurious emission	±2M offset		-35	-20	dBm
	>±3MHz offset		-40	-30	dBm

*The measurement does not include exceptions in these bands. Exceptions can pass Bluetooth SIG spec.
**The measurement is at chip output.

2.7 Crystal Oscillator

2.7.1 Reference Clock

A 26MHz crystal oscillator with one external 26MHz cock buffer and one 32kHz clock output is integrated in SOC.

The mode of operation will be detected automatically, which means if an external clock is detected, it will enter external 26MHz clock mode, otherwise it will enter 32kHz clock mode.

2.7.2 Reference Output Clock Buffers Specification (for PMIC MT6392)

Table 2-47: Reference output clock buffer specification

XMODE_TP2	26M CLOCK output buffer
Max. driving capability	30pF // 3K
Swing Vpp (Max./Min.)	1.2V/0.7V
Waveform	Square
PN requirement 5Hz	-73dBc/Hz (worst)
PN requirement 10Hz	-80 dBc/Hz (worst)
PN requirement 100Hz	-105 dBc/Hz (worst)
PN requirement 1kHz	-127 dBc/Hz (worst)
PN requirement 10kHz	-140 dBc/Hz (worst)
PN requirement 100kHz	-143 dBc/Hz (worst)

2.7.3 XTAL component characteristic specification for crystal oscillation mode

Table 2-48: XTAL component spec

XTAL characteristics	Specification
Frequency Tolerance@25deg	+-10ppm
Frequency Stability over temperature	+-10ppm
ESR	<300hm
CL	10.5pF~12.0pF
TS	10-15ppm/pF
DL	>100uW

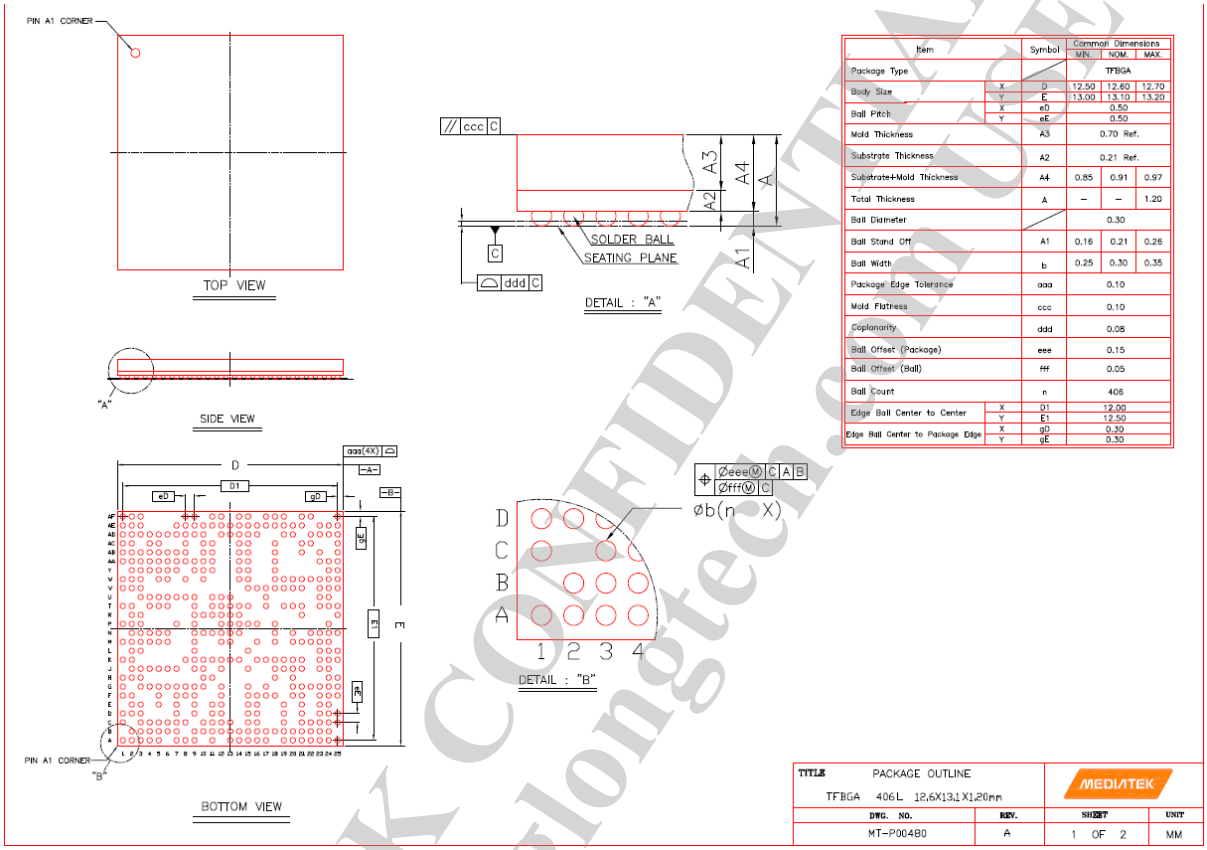
2.7.4 External reference clock oscillator specification

Table 2-49: External reference clock source specification

External reference clock(TCXO) characteristics	Specification
Max. driving capability	30pF // 3K
Swing Vpp (Max./Min.)	1.2V/0.7V
Waveform	Square
PN requirement 5Hz	<-83 dBc/Hz
PN requirement 10Hz	<-90 dBc/Hz
PN requirement 100Hz	<-115 dBc/Hz
PN requirement 1kHz	<-137 dBc/Hz
PN requirement 10kHz	<-150 dBc/Hz
PN requirement 100kHz	<-153 dBc/Hz

2.8 Package Information

2.8.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	12.50	12.60	12.70
	Y	E	13.00	13.10	13.20
Ball Pitch	X	eD		0.50	
	Y	eE		0.50	
Mold Thickness		A3		0.70 Ref.	
Substrate Thickness		A2		0.21 Ref.	
Substrate+Mold Thickness		A4	0.85	0.91	0.97
Total Thickness		A	–	–	1.20
Ball Diameter				0.30	
Ball Stand Off		A1	0.16	0.21	0.26
Ball Width		b	0.25	0.30	0.35
Package Edge Tolerance		aaa		0.10	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		406	
Edge Ball Center to Center	X	D1		12.00	
	Y	E1		12.50	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

DWG. NO.	REV.	SHEET	UNIT
MT-P004B0	A	1 OF 2	MM

Figure 2-22: Outlines and dimensions of TFBGA 12.6mm*13.1mm, 406-ball, 0.5mm pitch package

Table 2-50. Package Details

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	12.50	12.60	12.70
	Y	E	13.00	13.10	13.20
Ball Pitch	X	eD	0.50		
	Y	eE	0.50		
Mold Thickness		A3	0.70 Ref.		
Substrate Thickness		A2	0.21 Ref.		
Substrate+Mold Thickness		A4	0.85	0.91	0.97
Total Thickness		A	—	—	1.20
Ball Diameter			0.30		
Ball Stand Off		A1	0.16	0.21	0.26
Ball Width		b	0.25	0.30	0.35
Package Edge Tolerance		aaa	0.10		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	406		
Edge Ball Center to Center	X	D1	12.00		
	Y	E1	12.50		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

2.8.2 Thermal Operating Specifications

Table 2-51: Thermal operating specifications

Symbol	Description	Value	Unit	Notes
	Maximum operating junction temperature	105	°C	
	Package thermal resistances in nature convection	31.03	°C/Watt	

2.8.3 Lead-free Packaging

MT8516A is provided in a lead-free package and meets RoHS requirements.

2.9 Ordering Information

2.9.1 Top Marking Definition

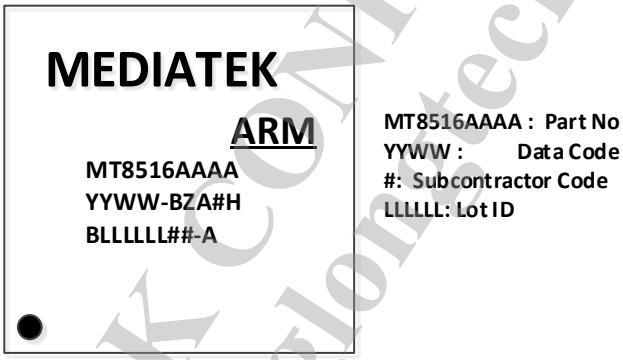


Figure 2-23: Top mark of MT8516A

2.9.2 Ordering Part Number

MT8516AAAA/B

